# MT7621 Programming Guide
## 7-port Gigabit Ethernet Switch

Version: 0.3
Release date: 2014-09-09

# Document Revision History

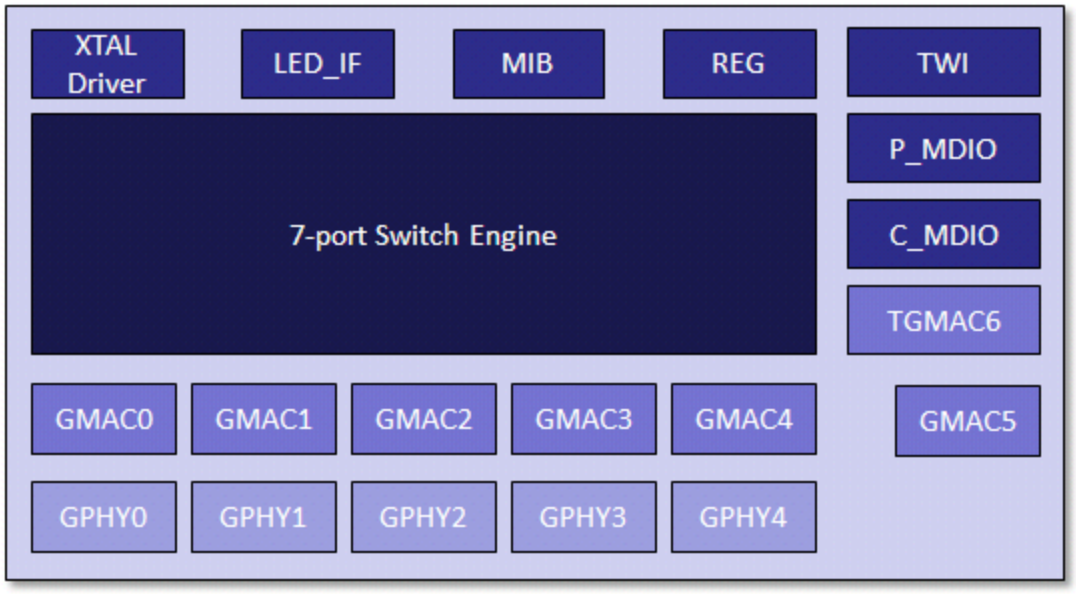
| Revision | Date | Author | Note |
|---|---|---|---|
| V01 | 2014/05/26 | PeterCT WU | Initial version |
| V02 | 2014/05/26 | PeterCT Wu | Source from 7530 |
| V03 | 2014/09/9 | PeterCT Wu | Add loop detection |
| V04 | 2014/10/16 | PeterCT Wu | Update QoS Setting |

# Table of Contents

# 1 General Description

## 1.1 Introduction

MT7621 GSW is a highly integrated Ethernet switch with high performance and non-blocking transmission. It includes a 7-port Gigabit Ethernet MAC and a 5-port Gigabit Ethernet PHY for several applications, such as xDSL, xPON, WiFi AP, and cable modem. MT7621 GSW enables an advanced power-saving feature to meet the market requirement. It complies with IEEE803.3az for Energy Efficient Ethernet and cable-length/link-down power saving mode. MT7621 GSW is also designed for cost-sensitive applications in retail and Telecom market. MediaTek's industry-leading techniques provide customers with the most cost-competitive and lowest power consumption Ethernet product in the industry. Please refer to the below figure to know the construct of MT7621 GSW.



# 2 Function Description

## 2.1 Mode setting

The register 0x 7800 is hardware trap, it is made when power on (define by boot-strap resistance). You can change it by writing 0x7804. Finally, the system would active according ox7804 not 0x7800. Some registers of 0x7800 cannot be changed. For detail, please check the switch register map. You should check it bit by bit.

**00007800 HWTRAP Hardware Trap Status Register 01007FFF**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |
| Type | | | | | | | | | | | | | | | | |
| Reset | | | | | | | | | | | | | | | | |
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | | ht_loopdet_dis | ht_p5_intf_sel | ht_smi_addr | | ht_xtal_fsel | | ht_p6_intf_dis | ht_p5_intf_mode | ht_p5_intf_dis | ht_c_mdio_bps_n | ht_eeprom_en | ht_chip_mode | | | |
| Type | | RO | RO | RO | | RO | | RO | RO | RO | RO | RO | RO | | | |
| Reset | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

If you want to change 0x7804, you need to set bit 16 as 1 of 0x7804 first.

**00007804 MHWTRAP Modified Hardware Trap Status Register 0100000F**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | csr_p5_phy0_sel | | | | csr_chg_trap |
| Type | | | | | | | | | | | | RW | | | | RW |
| Reset | | | | | | | | | | | | 0 | | | | 0 |
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | csr_gsw_ck_sel | csr_loopdet_dis | csr_p5_intf_sel | csr_smi_addr | | csr_xtal_fsel | | csr_p6_intf_dis | csr_p5_intf_mode | csr_p5_intf_dis | csr_c_mdio_bps_n | csr_eeprom_en | csr_chip_mode | | | |
| Type | RW | RW | RW | RO | | RO | | RW | RW | RW | RW | RO | RO | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 20 | csr_p5_phy0_sel | **When p5_intf_sel == 1'b0, the external device will be connected to**<br>1'b0: GPHY4<br>1'b1: GPHY0 |
| 16 | csr_chg_trap | **Change HW-TRAP setting**<br>1'b1: Change<br>1'b0: Use default HW-TRAP setting |
| 15 | csr_gsw_ck_sel | **Control GSW_CK (if csr_chg_trap == 1)**<br>1'b0: 500MHz<br>1'b1: 200MHz |
| 14 | csr_loopdet_dis | **Hardware Loop Detection Disable (if csr_chg_trap == 1)**<br>1'b0: Enable<br>1'b1: Disable |
| 13 | csr_p5_intf_sel | **Port 5 Interface Selection (if csr_chg_trap == 1)**<br>1'b1: P5 Interface connects to GMAC5<br>1'b0: P5 Interface connects to GePHY4 or GePHY0 (depends on csr_p5_phy0_sel) |

| | | |
|---|---|---|
| 12:11 | csr_smi_addr | **csr_smi_addr is equal to ht_smi_addr[1:0] (offset: 0x7800, bit 12~11) since this hardware trap cannot be modified by software.** |
| 10:9 | csr_xtal_fsel | **csr_xtal_fsel is equal to ht_xtal_fsel[1:0](offset: 0x7800, bit 10~9)since this hardware trap cannot be modified by software.** |
| 8 | csr_p6_intf_dis | **From hw_trap[8]**<br>Port 6 Interface Disable (if csr_chg_trap == 1)<br>1'b0: Enable<br>1'b1: Disable |
| 7 | csr_p5_intf_mode | **Port 5 Interface Mode (if csr_chg_trap == 1)**<br>1'b0: GMII/MII<br>1'b1: RGMII |
| 6 | csr_p5_intf_dis | **Port 5 Interface Disable (if csr_chg_trap == 1)**<br>1'b1: Disable<br>1'b0: Enable |
| 5 | csr_c_mdio_bps_n | **Directly access phy mdc (if csr_chg_trap==1)**<br>0: Directly access PHY registers via C_MDC/C_MDIO<br>1: Indirectly access PHY registers |
| 4 | csr_eeprom_en | **csr_eeprom_en is equal to ht_eeprom_en (offset: 0x7800, bit 4) since this hardware trap cannot be modified by software.** |
| 3:0 | csr_chip_mode | **csr_chip_mode is equal to ht_chip_mode[3:0] (offset: 0x7800, bit 3~0) since this hardware trap cannot be modified by software.** |

Please also check the detail hardware strapping of GSW.

| Pin Name | Type | Pin Number | Description |
|---|---|---|---|
| P4_LED_0<br>P3_LED_0 | I/O | 99<br>102 | Crystal clock frequency selection<br>{P4_LED_0, P3_LED_0} signals are used to control the crystal clock input frequency to XO and XI.<br>00: Reserved.<br>01: 20MHz<br>10: 40MHz<br>11: 25MHz (default) |
| P3_LED_2<br>P3_LED_1 | I/O | 100<br>101 | SMI Address selection<br>{P3_LED_2, P3_LED_1} signals are used to define decoded Serial Management Interface(SMI) addresses of C_MDC/C_MDIO for command registers access<br>00 : Use 7 to 12 SMI addresses<br>01 : Use 15 to 20 SMI addresses<br>10 : Use 23 to 28 SMI addresses<br>11 : Use 31 and 0 to 4 SMI addresses (default) |
| P1_LED_1 | I/O | 107 | SMI Access control<br>0: PHY access mode 0<br>1: PHY access mode 1 (default) |
| P1_LED_2 | I/O | 106 | P5 Interface Disable<br>0: Enable P5 IO<br>1: Disable P5 IO (default) |

| Pin Name | Type | Pin Number | Description |
|---|---|---|---|
| P2_LED_1 | I/O | 104 | P5 Interface Mode<br>0: GMII or MII mode<br>1: RGMII mode (default) |
| P4_LED_1 | I/O | 98 | P5 Interface Selection<br>0: P5 IO is connected to GPHY4<br>1: P5 IO is connected to GMAC5 (default) |
| P2_LED_2 | I/O | 103 | P6 Interface Disable<br>0: Enable P6 IO<br>1: Disable P6 IO (default) |
| P0_LED_2 | I/O | 109 | EEPROM Auto Initialization<br>0: Disable EEPROM auto initialization<br>1: Enable EEPROM auto initialization (default) |
| P4_LED_2 | I/O | 97 | Loop Detection Alarm<br>0: Enable loop detection<br>1: Disable loop detection (default) |

*Note 1: We would suggest that SMI address of GSW is 5'b11111. If not, you need to change the driver of GSW.

## 2.2 Reset

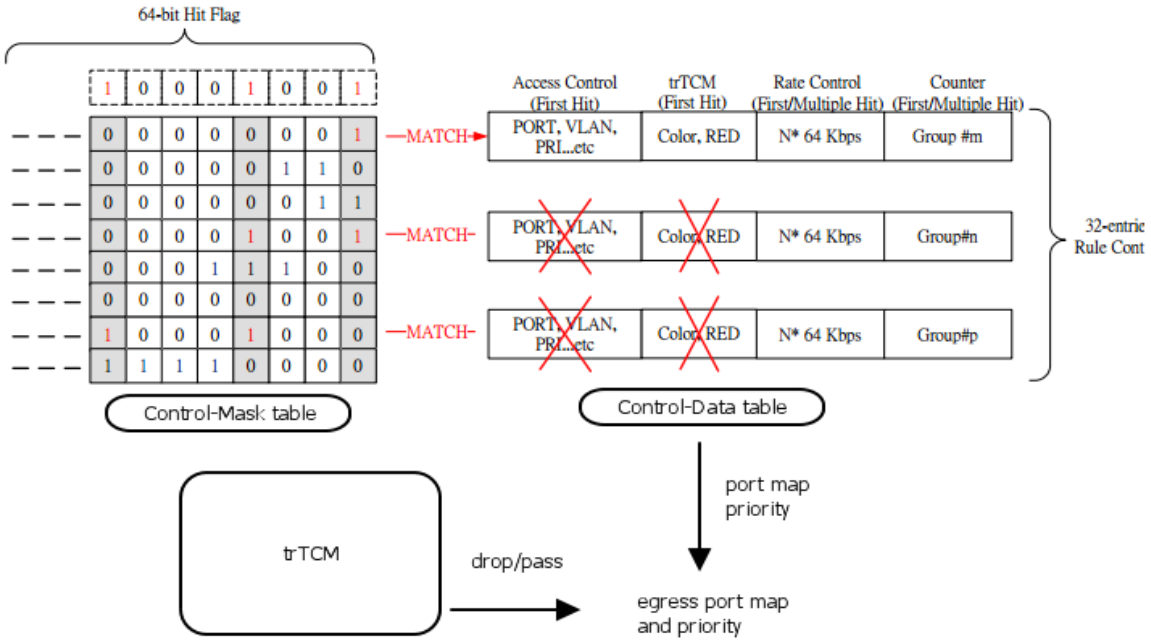
Check the Register 0x7000 if you want to do the software reset to switch or PHY. Usually, we would set 0x7000 as 0x3 for re-start switch.

**00007000 SYS_CTRL System Control 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | ACL_TAB_INIT | MAC_TAB_INIT | VLAN_TAB_INIT | | | | BMU_MEM_INIT |
| Type | | | | | | | | | | RO | RO | RO | | | | RO |
| Reset | | | | | | | | | | 0 | 0 | 0 | | | | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | TRTCM_BIST_STS | MASK_BIST_STS | CTRL_BIST_STS | ADDR_BIST_STS | VLN_BIST_STS | MIB_BIST_STS | PB_BIST_STS | PL_BIST_STS | FL_BIST_STS | MBIST_CMP | MBIST_EN | | SW_PHY_RST | SW_SYS_RST | SW_REG_RST |
| Type | | RO | RO | RO | RO | RO | RO | RO | RO | RO | RO | RW | | R/W/SC | R/W/SC | R/W/SC |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 |

## 2.3 Access control list (ACL)

ACL Rule table is implemented along with packet parser. For the incoming packet, 2-bytes packet content will be filtered sequentially and compared with 64 patterns in the ACL rule table. When one pattern is hit, the corresponding rule flag will be set. After the whole packet is done, the final 64-bits rule flag will be sent to the ACL look-up engine to get the corresponding rule control. GSW can support up to 32 entries ACL rules.




Take port 0 for example:
0x2004 ff0400 //enable ACL of port 0, this setting is by per-port.

After enable ACL, you need to setup ACL hit pattern. We would check the VLAN for example here.

**First:**

**Set ACL pattern:**

0x94 ffff8100 //"ffff" mean compare 2-bytes payload and need match 0x8100.
0x98 0008ff0c //ACL pattern enable, MAC header. P0 to P6. Offset 12byte.
0x90 80005001 //bit [15:12]: 4'b0101:
//Write the specific ACL Table entry. It is 1st rule.

**Second:**

**Set ACL mask:**

0x94 00000021 //0x21 = 0010.0001 . Active 1st and 6th rule.

0x98 00000000
0x90 80009002 //bit [15:12]: 4'b1001: Write the specific 3rd ACL Mask entry
//use mask can enable many rules at the same time

**Or set ACL mask (another sample):**
0x94 00000004 //0x4= 0100. Active 3th rule.
0x98 80000000 //0x80000000= 1000.0000.0000.0000 . Active 63th rule.
0x90 8000903F //bit [15:12]: 4'b1001: Write the specific 64th ACL Mask entry
//The first Mask start from "0", so the 64th mask entry is 0x3f(63).

**Setup the ACL action:**
0x94 18000080 //Refer to 0x0094 (ACL rule control). This is used for drop packet.
0x98 00000000
0x90 8000b001 //bit [15:12]: 4'b1011: Write ACL rule control entry, Action for 1st rule.
//The first rule entry need to start from "1".

| Destination Address | Source Address | VLAN TAG | Type / Length | Payload | FCS |
|---|---|---|---|---|---|
| 6 byte | 6 byte | 4byte | 2byte | 1500 byte | 4 byte |

**00002004** PCR **Port Control of P0** **00FF0000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | MLDv2_EN | EG_TAG | | REV1 | PORT_PRI | | | PORT_MATRIX | | | | | | | |
| Type | DC | RW | RW | | DC | RW | | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | REV2 | | | UP2DSCP_EN | UP2TAG_EN | ACL_EN | PORT_TX_MIR | PORT_RX_MIR | ACL_MIR | MIS_PORT_FW | | | REV3 | VLAN_MIS | PORT_VLAN | |
| Type | DC | | | RW | RW | RW | RW | RW | RW | RW | | | DC | RW | RW | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**00000090** VTCR **VLAN Table Control** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | BUSY | REV0 | | | | | | | | | | | | | | IDX_INVLD |
| Type | W1C | DC | | | | | | | | | | | | | | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FUNC | | | | VID | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | BUSY | **VLAN Table Is Busy**<br>SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC |

| | | |
|---|---|---|
| | | bits. |
| 30:17 | REV0 | **Reserved** |
| 16 | IDX_INVLD | **Entry is not Valid**<br>This index for the access control is out of the valid index. |
| 15:12 | FUNC | **Access Control Function**<br>Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.<br>4'b0000: Read the specified VID Entry from VAWD# register based on VID bits<br>4'b0001: Write the specified VID Entry though VAWD# register based on VID bits.<br>4'b0010: Make the specified VID entry invalid based on VID bits.<br>4'b0011: Make the specified VID entry valid based on VID bits .<br>4'b0100: Read the specified ACL Table entry.<br>4'b0101: Write the specified ACL Table entry.<br>4'b0110: Read the specified trTCM Meter Table.<br>4'b0111: Write the specified trTCM Meter Table.<br>4'b1000: Read the specified ACL Mask entry.<br>4'b1001: Write the specified ACL Mask entry.<br>4'b1010: Read the specified ACL Rule Control entry.<br>4'b1011: Write the specified ACL Rule Control entry.<br>4'b1100: Read the specified ACL Rate Control entry.<br>4'b1101: Write the specified ACL Rate Control entry.<br>4'b1110: Reserved<br>4'b1111: Reserved |
| 11:0 | VID | **1. VLAN ID Number: 0x0 to 0x1F (16)**<br>2. ACL table index: 0x0 to 0x3F (64)<br>3. ACL mask control: 0x0 to 0x3F (32 or 64) |

## 0x94

(ACL Rule Table)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:16 | RW | BIT_MASK | **Comparison Pattern Mask** | 0x0 |
| 15:0 | RW | CMP_PAT | **Comparison Pattern** | 0x0 |

(ACL Rule Mask)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:0 | RW | ACL_MASK | **ACL Mask[31:0]** | 0x0 |

(ACL Rule Control)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:30 | - | - | Reserved | 0x0 |
| 29 | RW | ACL_MANG | Management Frame Attribute | 0x0 |
| 28 | RW | INT_EN | Interrupt Enable | 0x0 |
| 27 | RW | ACL_CNT_EN | Enable ACL Hit Count | 0x0 |
| 26:24 | RW | CNT_IDX | Counter Group Index | 0x0 |
| 23 | RW | VLAN_PORT_EN | Swap VLAN Member | 0x0 |
| 22 | RW | DA_SWAP | Multicast MAC Address Swap | 0x0 |
| 21 | RW | SA_SWAP | Source MAC Address Swap | 0x0 |
| 20 | RW | PPP_RM | PPPoE Header Removal | 0x0 |
| 19 | RW | LKY_VLAN | Leaky VLAN | 0x0 |
| 18:16 | RW | EG_TAG | Egress VLAN Tag Attribute | 0x0 |
| 15:8 | RW | PORT | Destination Port / VLAN Member | 0x0 |
| 7 | RW | PORT_EN | Force Destination port | 0x0 |
| 6:4 | RW | PRI_USER | User Priority from ACL | 0x0 |
| 3 | RW | MIR_EN | Frame Copy to Mirror Port | 0x0 |
| 2:0 | RW | PORT_FW | Frame TO_CPU Forwarding | 0x0 |

**0x98**

(ACL Rule Table)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:20 | - | - | Reserved | 0x0 |
| 19 | RW | EN | ACL Pattern Enable | 0x0 |
| 18:16 | RW | OFST_TP | Offset Range | 0x0 |
| 15:8 | RW | SP | Incoming Source Port Bit-map | 0x0 |
| 7:1 | RW | WORD_OFST | Word Offset | 0x0 |
| 0 | RW | CMP_SEL | Comparison mode selection | 0x0 |

**Offset range table:**

3'b000: MAC Header (inc. VLAN tags and Length/Type) (L2 Offset)
3'b001: L2 Payload (L2 Offset)
3'b010: IP Header (L3 Offset)
3'b011: IP Datagram (L3 Offset)

3'b100: TCP/UDP Header (L4 Offset)
3'b101: TCP/UDP Datagram (L4 Offset)
3'b110: IPv6 Header (L3 Offset)
3'b111: Reserved

(ACL Rule Mask)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:0 | RW | ACL_MASK | ACL Mask[63:32] | 0x0 |

(ACL Rule Control)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:24 | RW | Reserved | | 0x0 |
| 23:19 | RW | ACL_CLASS_IDX | **Class index for the 32-entries meter table** | 0x0 |
| 18:17 | RW | Reserved | | 0x0 |
| 16 | RW | Reserved | | 0x0 |
| 15:14 | RW | Reserved | | 0x0 |
| 13:11 | RW | DROP_PCD_G | **User Defined Drop Precedence for Green color packet** | 0x0 |
| 10:8 | RW | DROP_PCD_Y | **User Defined Drop Precedence for Yellow color packet** | 0x0 |
| 7:5 | RW | DROP_PCD_R | **User Defined Drop Precedence for Red color packet** | 0x0 |
| 4:2 | RW | CLASS_SLR | **User Defined Class Selector** | 0x0 |
| 1 | RW | CLASS_SLR_SEL | **Select original class_selector value or ACL control table defined class selector value** | 0x0 |
| 0 | RW | DROP_PCD_SEL | **Select original drop precedence value or ACL control table defined drop Precedence value** | 0x0 |

## 2.4 Broadcast Storm suppression

Broadcast Storm is commonly caused by faulty protocol implementations, undetected network loops, or faulty network equipment. Broadcast storms can cause significant disruption to the network. Broadcast control is possible by using filters or user-defined throttle settings that limit broadcast/multicast propagation to a certain rate.
GSW provide the per-port broadcast storm controller , loop detection and alarm signal to avoid it. Here we show the example to do the rate-base control of Broadcast storm.

Register 0x30c0 is used for setting the loop detection.

You may set it if Broadcast storm came from port 1:
Set 0x30c0 as 0x1f130000 //port 0 ~ port 4 enable LPDET,
Set 0x211c as 0xce030303 //set port 1 to detect broadcast storm according to rate-based , and drop the packet. The limit rate is around 3Mbps for 1000Mbps, 100Mbps and 10Mbps base.

Read 0x30c0 again to check the per-port LPDET_ALARMx information.

**000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | LPDET_EN6 | LPDET_EN5 | LPDET_EN4 | LPDET_EN3 | LPDET_EN2 | LPDET_EN1 | LPDET_EN0 | LPDET_PERIOD_EN | LPDET_ALARM_EN | LPDET_PASS | LPDET_PERIOD | LPDET_LED_RATE | LPDET_THRESHOLD | | |
| Type | | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LPDET_ST_LOOP | LPDET_ST_BCST | LPDET_TRAP_EN | | | | | | | LPDET_ALARM6 | LPDET_ALARM5 | LPDET_ALARM4 | LPDET_ALARM3 | LPDET_ALARM2 | LPDET_ALARM1 | LPDET_ALARM0 |
| Type | RO | RO | RO | | | | | | | RO | RO | RO | RO | RO | RO | W1C |
| Reset | 0 | 0 | 0 | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 30 | LPDET_EN6 | **Enable the loop detection ability of user port 6.**<br>0: Disable<br>1: Enable |
| 29 | LPDET_EN5 | **Enable loop detection the ability of user port 5.**<br>0: Disable<br>1: Enable |
| 28 | LPDET_EN4 | **Enable loop detection the ability of user port 4.**<br>0: Disable<br>1: Enable |
| 27 | LPDET_EN3 | **Enable loop detection the ability of user port 3.**<br>0: Disable<br>1: Enable |
| 26 | LPDET_EN2 | **Enable loop detection the ability of user port 2.**<br>0: Disable<br>1: Enable |
| 25 | LPDET_EN1 | **Enable loop detection the ability of user port 1.**<br>0: Disable<br>1: Enable |
| 24 | LPDET_EN0 | **Enable loop detection the ability of user port 0.**<br>0: Disable<br>1: Enable |
| 23 | LPDET_PERIOD_EN | **The loop detection frame is triggered by a periodical timer or by broadcast storm.**<br>0: Broadcast mode<br>1: Periodical mode |
| 22 | LPDET_ALARM_EN | **Enable 2 kHz alarm output and per-port LED when loop is detected.**<br>0: Disable<br>1: Enable |

| | | |
|---|---|---|
| 21 | LPDET_PASS | **Loop detection frame is blocked or passed to packet memory.**<br>0: Blocked<br>1: Pass |
| 20 | LPDET_PERIOD | **Interval of transmitting loop detection frame in Periodical mode.**<br>0: 125 us<br>1: 1000 ms |
| 19 | LPDET_LED_RATE | **LED blinking rate of per port when loop is detected.**<br>0: LED blinking at 2 Hz<br>1: LED blinking at 4 Hz |
| 18:16 | LPDET_THRESHOLD | **Number of missed loop detection frame before 2 kHz alarm is reset** |
| 15 | LPDET_ST_LOOP | **The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.**<br>0: Not in Loop state<br>1: Loop state |
| 14 | LPDET_ST_BCST | **The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.**<br>0: Not in BCST state<br>1: BCST state |
| 13 | LPDET_TRAP_EN | **Status of strap pin for loop detection**<br>0: Disabled<br>1: Enabled |
| 6 | LPDET_ALARM6 | **The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 5 | LPDET_ALARM5 | **The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 4 | LPDET_ALARM4 | **The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 3 | LPDET_ALARM3 | **The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 2 | LPDET_ALARM2 | **The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 1 | LPDET_ALARM1 | **The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 0 | LPDET_ALARM0 | **The status of loop detected on port 0. This bit is cleared when it is written as 1.**<br>0: Not detected<br>1: Detected |

**0000201C BSR Broadcast Storm Rate Control of P0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | STRM_MODE | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT | | STORM_1G | | | | | | | |
| Type | RW | RW | RW | RW | RW | RW | RW | | RW | | | | | | | |

| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | STORM_100M | | | | | | | | STORM_10M | | | | | | | |
| Type | RW | | | | | | | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | STRM_MODE | **Broadcast Storm Suppression**<br>0: Packet-based ( 1 second period)<br>1: Rate-based |
| 30 | STRM_BC_INC | **Broadcast Storm Included**<br>0: Exclude BC frame<br>1: Include BC frame |
| 29 | STRM_MC_INC | **Unknown Multicast Storm Included**<br>0: Exclude MC frame<br>1: Include MC frame |
| 28 | STRM_UC_INC | **Unknown Unicast Storm Included**<br>0: Exclude UC frame<br>1: Include UC frame |
| 27 | STRM_DROP | **Broadcast Storm Suppression enabled**<br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected |
| 26 | STRM_PERD | **Broadcast Strom Detection Signal Period**<br>0: One second<br>1: 125us |
| 25:24 | STRM_UNIT | **Broadcast Storm Suppression**<br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16 | STORM_1G | **1000 Mbps Broadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 1000 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |
| 15:8 | STORM_100M | **100 Mbps Broadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 100 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bp |
| 7:0 | STORM_10M | **10 MbpsBroadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 10 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |

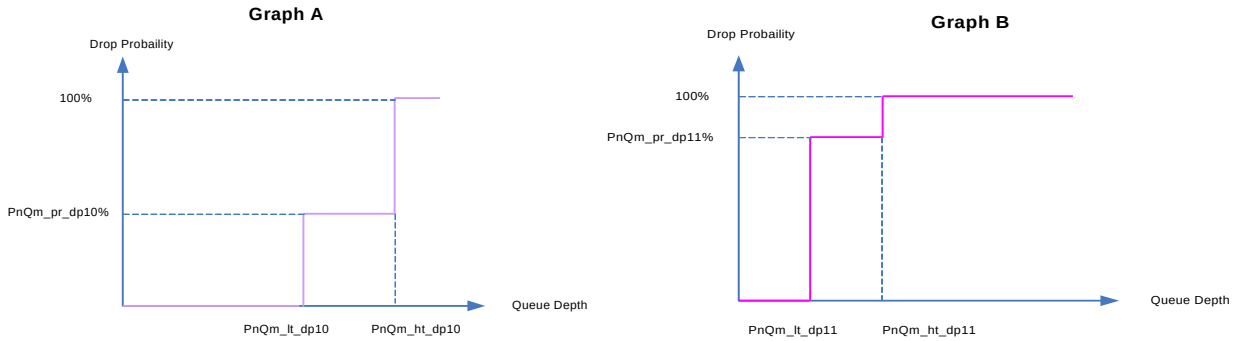
## 2.5 Drop Precedence control

The “Drop Precedence” is addon function for the Flow Control. The function can enable or disable. When an enqueue request is on, the control signals of the packet like as queue priority, drop precedence which are from ARL module will feed into Drop Precedence controller, the controller will check the queue depth and drop probability to decide the packet will be dropped or not. Fin ally, it will feedback the “dp_packet_drop”

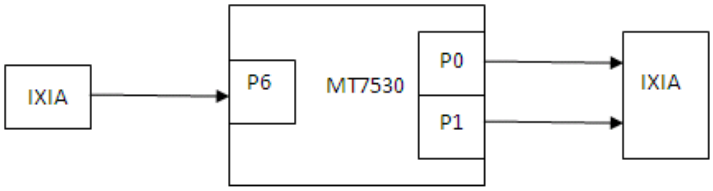
signal to tell the Flow Control to drop the packet or not. The drop precedence of value is by user setting inthe ACL entry or trTCM engine.

The meaning of dorop precedence which is from ARL is
(a) 2'b00, 2'b01 : No drop.
(b) 2'b10 : The drop probability of the incoming packet is based on "Graph A" setting.
(c) 2'b11 : The drop probability of the incoming packet is based on "Graph B" setting.

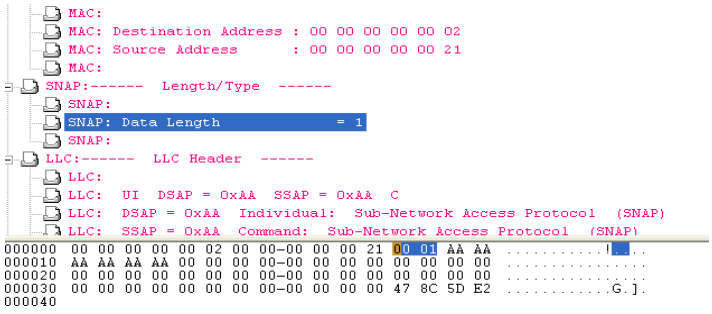
PnQm_pr_dp10/11 : Drop probability of Port n Queue m when drop precedence = 2'b10/2'b11.
PnQm_lt_dp10/11 : Low threshold of of Port n Queue m when drop precedence = 2'b10/2'b11.
PnQm_ht_dp10/11 : High threshold of of Port n Queue m when drop precedence = 2'b10/2'b11.




Here we show the test environment as below:




We would design one ACL to hit the"0x0001" in the data from port 6 to mark a color for it. And use DROP precedence at port 0.




;ACL port enable

```
ethphxcmd gsww 2604 00ff0403

;ACL entry
ethphxcmd gsww 0094 ffff0001        // 0xffff - compare 2-byte data
                                    // 0x0001- compare pattern should be as 0x0001

ethphxcmd gsww 0098 0008400c        // 0x000 MAC offset (bit 18:16)
                                    //0x8 – ACL pattern enable
                                    // 0x4 – incoming source port is port 6(bit 15:8)
                                    // 0xc –offset
ethphxcmdgsww 0090 80005000         //Write ACL table entry

ethphxcmd gsww 0094 00000001
ethphxcmd gsww 0098 00000000
ethphxcmd gsww 0090 80009000       //Write ACL mask

ethphxcmd gsww 0094 00000000
ethphxcmd gsww 0098 00060000       //mark as red
ethphxcmd gsww 0090 8000b000       //ACL rule control
```

- Set Drop precedence for Port 0 Q2

```
ethphxcmd gsww 180c 80000000  //enable drop precedence
ethphxcmd gsww 1814 80000000
ethphxcmd gsww 182c 011ff000    // Drop probability of P0 Q2
```

0x0098 (ACL Rule Control)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:24 | RW | Reserved | | 0x0 |
| 23:19 | RW | ACL_CLASS_IDX | ACL Class index for the 32-entries meter table (TrTcm) | 0x0 |
| 18:17 | RW | ACL_ User defined color remark | 00:default, 01:Green, 10:Yellow, 11:Red) | 0x0 |
| 16 | RW | Select Color | 1: TrTcm<br>0: ACL | 0x0 |
| 15:14 | RW | Reserved | | 0x0 |
| 13:11 | RW | DROP_PCD_G | User Defined Drop Precedence for Green | 0x0 |
| 10:8 | RW | DROP_PCD_Y | User Defined Drop Precedence for Yellow | 0x0 |
| 7:5 | RW | DROP_PCD_R | User Defined Drop Precedence for Red | 0x0 |
| 4:2 | RW | CLASS_SLR | User Defined Class Selector | 0x0 |

| | | | | |
|---|---|---|---|---|
| 1 | RW | CLASS_SLR_SEL | Select ACL Defined Class Selector | 0x0 |
| 0 | RW | DROP_PCD_SEL | Select ACL Defined Drop Precedence | 0x0 |

**0000180C MMDPR_10_Q0P0 Drop Precedence control 10 of Q0 Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | P0_DP_en | | | | | P0Q0_pr_dp10 | | | | | | P0Q0_ht_dp10[8:4] | | | | |
| Type | RW | | | | | RW | | | | | | RW | | | | |
| Reset | 0 | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | P0Q0_ht_dp10[3:0] | | | | | | | P0Q0_lt_dp10 | | | | | | | | |
| Type | RW | | | | | | | RW | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | P0_DP_en | **Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF)**<br>**(1) When queue depth >= P0Q0_ht_dp10, the drop probability of the incoming packet is 100%.**<br>(2) When queue depth < P0Q0_lt_dp10, the drop probability of the incoming packet is 0%.<br>(3) When P0Q0_lt_dp10 <= queue depth < P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10.<br>0: Disable<br>1: Enable |
| 26:24 | P0Q0_pr_dp10 | **Drop probability of P0 Q0 for drop precedence = 2'b10.**<br>0x0: 0%<br>0x1: 12.5%<br>0xn: n* 12.5%<br>0x7: 87.5%<br>(n=2~6) |
| 20:12 | P0Q0_ht_dp10 | **High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size** |
| 8:0 | P0Q0_lt_dp10 | **Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size** |

**00001814 MMDPR_10_Q2P0 Drop Precedence control 10 of Q2 Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | P0Q2_pr_dp10 | | | | | | P0Q2_ht_dp10[8:4] | | | | |
| Type | | | | | | RW | | | | | | RW | | | | |
| Reset | | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | P0Q2_ht_dp10[3:0] | | | | | | | P0Q2_lt_dp10 | | | | | | | | |
| Type | RW | | | | | | | RW | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 26:24 | P0Q2_pr_dp10 | **Drop probability of P0 Q2 for drop precedence = 2'b10.**<br>0x0: 0%<br>0x1: 12.5%<br>0xn: n* 12.5% |

| | | |
|---|---|---|
| | | 0x7: 87.5%<br>(n=2~6) |
| 20:12 | P0Q2_ht_dp10 | **High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size** |
| 8:0 | P0Q2_lt_dp10 | **Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size** |

**0000182C** **MMDPR_11_Q0P0** **Drop Precedence control 11 of Q0 Port 0** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | P0Q0_pr_dp11 | | | | | | P0Q0_ht_dp11[8:4] | | | | |
| Type | | | | | | RW | | | | | | RW | | | | |
| Reset | | | | | | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | P0Q0_ht_dp11[3:0] | | | | | | | P0Q0_lt_dp11 | | | | | | | | |
| Type | RW | | | | | | | RW | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 26:24 | P0Q0_pr_dp11 | **Drop probability of P0 Q0 for drop precedence = 2'b11.**<br>0x0: 0%<br>0x1: 12.5%<br>0xn: n* 12.5%<br>0x7: 87.5%<br>(n=2~6) |
| 20:12 | P0Q0_ht_dp11 | **High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size** |
| 8:0 | P0Q0_lt_dp11 | **Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size** |

## 2.6 Egress Rate limit control

There are many ways to do the rate control, like ACL rate control, ingress or egress rate control. If you want to use egress rate control, please disable flow control first to avoid the ingress congestion.

Set bit 31 of 0x1fe0 as 0 to disable global flow control.
Set 0x10e0 as 0x118 to include the IPG byte for egress rate control.
Here we show the sample for port 1 egress rate control.

| egress rate | Reg 0x1140 |
|---|---|
| 10Mbps | 0x0138898f |
| 20Mbps | 0x0271898f |
| 30Mbps | 0x03a9898f |
| 40Mbps | 0x04e2898f |
| 100Mbps | 0x0c35898f |

**000010E0** **GERLCR** **Global Egress Rate Limit Control Register** **00000104**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |

| Type | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | | | | EGC_MFRM_EX | EGC_IPG_OP | EGC_IPG_BYTE | | | | | | | |
| Type | | | | | | | RW | RW | RW | | | | | | | |
| Reset | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 9 | EGC_MFRM_EX | **When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)**<br>0: Include management frames<br>1: Exclude management frames |
| 8 | EGC_IPG_OP | **Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.**<br>0: IPG byte is excluded<br>1: IPG byte is included |
| 7:0 | EGC_IPG_BYTE | **Egress Rate IPG Byte Count**<br>Byte count should be added while calculating the rate limit.<br>0x04: 4 byte CRC (default)<br>0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble |

## 00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | EGC_RATE_CIR_15_0_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | EG_RATE_LIMIT_EN_P0 | | | EGC_RATE_CIR_16_P0 | EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0 | | | | EGC_TB_EN_P0 | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 | | | | | | |
| Type | RW | | | RW | RW | | | | RW | RW | | | | | | |
| Reset | 0 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:16 | EGC_RATE_CIR_15_0_P0 | **Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps** |
| 15 | EG_RATE_LIMIT_EN_P0 | **EXP: egress_rate_limit_exp**<br>MAN: egress_rate_limit_man<br>Egress port rate limitation: MAN*10^(EXP)*1Kbps<br>0: Egress rate limit control disable<br>1: Enable |
| 12 | EGC_RATE_CIR_16_P0 | **Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value** |
| 11:8 | EG_RATE_LIMIT_EXP_P0 _EGC_TB_T_P0 | **Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),**<br>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement,<br>0: 1/128ms<br>1: 1/64ms<br>2: 1/32ms<br>3: 1/16ms<br>4: 1/8ms<br>5: 1/4ms<br>6: 1/2ms |

| | | |
|---|---|---|
| | | 7: 1ms<br>8: 2ms<br>9: 4ms<br>10: 8ms<br>11: 16ms<br>12: 32ms<br>13: 64ms<br>14: 128ms<br>15: 128ms |
| 7 | EGC_TB_EN_P0 | **When this bit is disabled, the Egress rate control acts like a leaky bucket principle.**<br>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.<br>0: CIR/CBS mode token bucket Disable<br>1: Token bucket mode Enable |
| 6:0 | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 | **Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),**<br>when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max ( EGC_CIR*EGC_TB_T, EGC_TB_CBS*512 ) |

## 2.7 Flow control

You should set 0x1fe0 bit 31 as 1 for global flow control first.

We take Port 5 for example, if you want to disable TX and RX flow control, you should set the bit 5 and bit 4 of 0x3500 as 0. And read 4th and 5th bit of 0x3508 to check it works or not.

Please know we just discussed about the MAC layer flow control. You need to check the PHY ability if you use auto polling mode. Please check the blow table:

| Local device | | Link partner | | Local device resolution | Link partner resolution |
|---|---|---|---|---|---|
| PAUSE | ASM_DIR | PAUSE | ASM_DIR | | |
| 0 | 0 | Don't care | Don't care | Disable PAUSE<br>Transmit and Receive | Disable PAUSE<br>Transmit and Receive |
| 0 | 1 | 0 | Don't care | Disable PAUSE<br>Transmit and Receive | Disable PAUSE<br>Transmit and Receive |
| 0 | 1 | 1 | 0 | Disable PAUSE<br>Transmit and Receive | Disable PAUSE<br>Transmit and Receive |
| 0 | 1 | 1 | 1 | Enable PAUSE transmit<br>Disable PAUSE receive | Enable PAUSE receive<br>Disable PAUSE transmit |
| 1 | 0 | 0 | Don't care | Disable PAUSE<br>Transmit and Receive | Disable PAUSE<br>Transmit and Receive |
| 1 | Don't care | 1 | Don't care | Enable PAUSE<br>Transmit and Receive | Enable PAUSE<br>Transmit and Receive |
| 1 | 1 | 0 | 0 | Disable PAUSE<br>Transmit and Receive | Disable PAUSE<br>Transmit and Receive |
| 1 | 1 | 0 | 1 | Enable PAUSE receive<br>Disable PAUSE transmit | Enable PAUSE transmit<br>Disable PAUSE receive |

**00001FE0 GFCCR0 Global Flow_Control Control Register 0 A0087858**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | FC_EN | | FC_OFF2ON_OPT | FC_ON2OFF_OPT | | | | | FC_PORT_BLK_THD | | | | | | | |
| Type | RW | | RW | RW | | | | | RW | | | | | | | |

| Reset | 1 | | 1 | 0 | | | | | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FC_FREE_BLK_HITHD | | | | | | | | FC_FREE_BLK_LOTHD | | | | | | | |
| Type | RW | | | | | | | | RW | | | | | | | |
| Reset | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | FC_EN | 0: Disable flow control<br>1: Enable flow control |
| 29 | FC_OFF2ON_OPT | **Flow control assertion option**<br>0: Disable<br>1: Enable aggressive frame discard option in flow control transition from OFF to ON |
| 28 | FC_ON2OFF_OPT | **Flow control de-assertion option**<br>0: Disable<br>1: Enable aggressive frame discard option in flow control transition from ON to OFF |
| 23:16 | FC_PORT_BLK_THD | **Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)** |
| 15:8 | FC_FREE_BLK_HITHD | **High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.** |
| 7:0 | FC_FREE_BLK_LOTHD | **Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block) See TBD.** |

## 00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | IPG_CFG_P5 | | EXT_PHY_P5 | MAC_MODE_P5 |
| Type | | | | | | | | | | | | | RW | | RW | RW |
| Reset | | | | | | | | | | | | | 0 | 1 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FORCE_MODE_P5 | MAC_TX_EN_P5 | MAC_RX_EN_P5 | | MAC_PRE_P5 | | BKOFF_EN_P5 | BACKPR_EN_P5 | FORCE_EEE1G_P5 | FORCE_EEE100_P5 | FORCE_RX_FC_P5 | FORCE_TX_FC_P5 | FORCE_SPD_P5 | | FORCE_DPX_P5 | FORCE_LNK_P5 |
| Type | RW | RW | RW | | RW | | RW | RW | RW | RW | RW | RW | RW | | RW | RW |
| Reset | 0 | 1 | 1 | | 0 | | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

## 00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

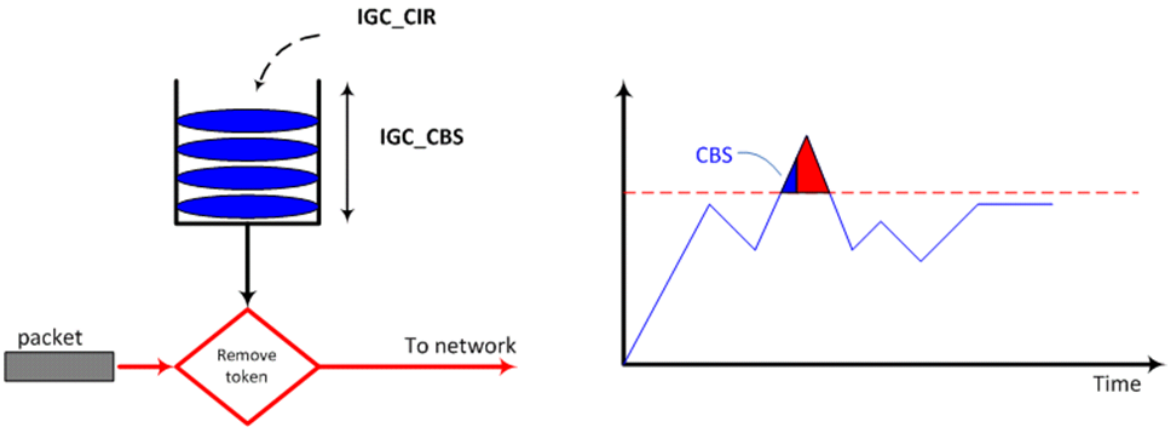
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |
| Type | | | | | | | | | | | | | | | | |
| Reset | | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | | | | | | EEE1G_STS_P5 | EEE100_STS_P5 | RX_FC_STS_P5 | TX_FC_STS_P5 | MAC_SPD_STS_P5 | | MAC_DPX_STS_P5 | MAC_LNK_STS_P5 |
| Type | | | | | | | | | RO | RO | RO | RO | RO | | RO | RO |
| Reset | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|

| | | |
|---|---|---|
| 7 | EEE1G_STS_P5 | **PORT 5 LPI Mode Status For 1000Mbps**<br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps<br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps |
| 6 | EEE100_STS_P5 | **PORT 5 LPI Status Mode For 100Mbps**<br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps<br>1: Capable of entering EEE Low Power Idle mode for 100Mbps |
| 5 | RX_FC_STS_P5 | **PORT 5 RX XFC Status. Port 5 Rx flow control status**<br>0: Disabled.<br>1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode. |
| 4 | TX_FC_STS_P5 | **PORT 5 TX XFC Status**<br>PORT 5 TX flow control status<br>0: Disabled.<br>1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2 | MAC_SPD_STS_P5 | **PORT 5 Speed [1:0] Status**<br>Current speed of PORT 5 after PHY links up.<br>00: 10 Mbps<br>01: 100 Mbps<br>10: 1000 Mbps<br>11: Reserved |
| 1 | MAC_DPX_STS_P5 | **PORT 5 duplex Status**<br>Current duplex mode of port 5 after PHY links up<br>0: Half Duplex<br>1: Full Duplex |
| 0 | MAC_LNK_STS_P5 | **Port 5 Link Up Status. Link up status of PORT 5.**<br>0: Link Down<br>1: Link Up |

## 2.8 Ingress rate control

Ingress rate control is one of basic rate control. We cannot limit the rate of physical transmission line, but we can limit the resources of packet process rate.
Refer to the below to know the behavior of ingress rate control:




-Each interval of time (programmable) H/W fill IGC_CIR bit token to bucket.

-H/W remove token (equal to packet size) when there is packet income.
-if remain token > packet, the packet can pass to network otherwise will drop packet.
-A bucket with CBS sizes allow some burst traffic pass switch.

For example, to set the ingress rate as 1000kbps
EGC_TBEN = 1
EGC_CIR = 1000K/32K = 31 = 0x1f
EGC_TB_T = ¼ ms

To avoid the inter-fame gap effect, please set 0x1ff0 as 0x00110118
We provide some reference data to do the rate control. For port 1, please set the register 0x1800.

| Ingress CIR | Reg 0x1800 |
|---|---|
| 10Mbps | 0x0138898f |
| 20Mbps | 0x0271898f |
| 30Mbps | 0x03a9898f |
| 40Mbps | 0x04e2898f |
| 100Mbps | 0x0c35898f |

**00001FF0 GIRLCR Global Ingress Rate Limit Control Register 00110104**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | IGC_FC_OFF_THD | | | | IGC_FC_DROP_THD | | | |
| Type | | | | | | | | | RW | | | | RW | | | |
| Reset | | | | | | | | | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | | | | IGC_MFRM_EX | IGC_IPG_OP | IGC_IPG_BYTE | | | | | | | |
| Type | | | | | | | RW | RW | RW | | | | | | | |
| Reset | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 23:20 | IGC_FC_OFF_THD | **Ingress Rate Limit Pause-Off Threshold**<br>Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold.<br>Threshold = max_bucket_size >> igc_fc_off_thd |
| 19:16 | IGC_FC_DROP_THD | **Ingress Rate Limit Drop Threshold**<br>If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold.<br>Threshold = -(max_bucket_size >> igc_fc_drop_thd) |
| 9 | IGC_MFRM_EX | **Ingress Rate Excludes Management Frames**<br>Management frames will be ignored by rate limit.<br>(management frame type is set by ARL registers)<br>0: Include management frames<br>1: Exclude management frames |
| 8 | IGC_IPG_OP | **Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation.**<br>0: IPG byte is excluded<br>1: IPG byte is included |
| 7:0 | IGC_IPG_BYTE | **Ingress Rate IPG Byte Count**<br>Byte count should be added while calculating the rate limit<br>8'h4: add 4 byte CRC (byte rate calculation) |

8'h18: add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation)

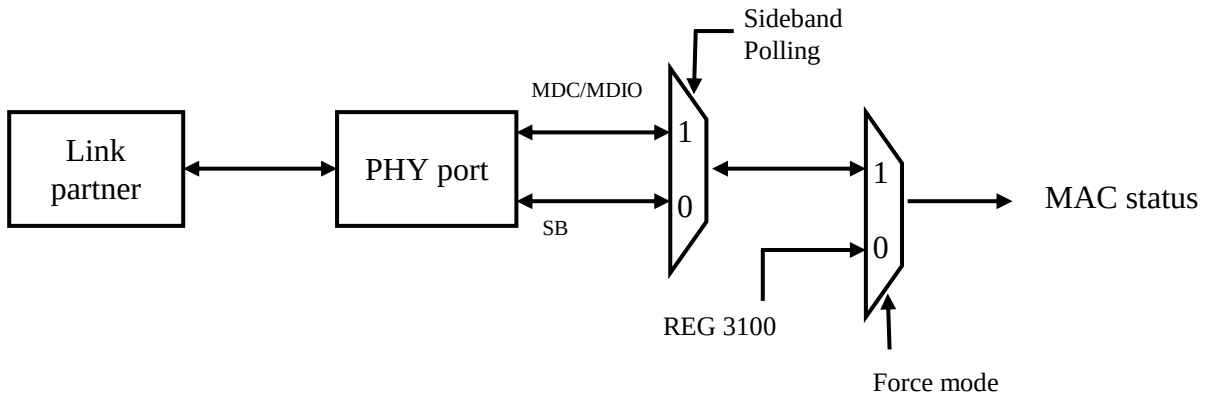
**00001800 IRLCR_P0 Ingress Rate Limit Control Register of Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | IGC_RATE_CIR_15_0_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IGC_RATE_EN_P0 | | | IGC_RATE_CIR_16_P0 | IGC_RATE_EXP_P0_IGC_TB_T_P0 | | | | IGC_TB_EN_P0 | IGC_RATE_MAN_P0_IGC_TB_CBS_P0 | | | | | | |
| Type | RW | | | RW | RW | | | | RW | RW | | | | | | |
| Reset | 0 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:16 | IGC_RATE_CIR_15_0_P0 | **Total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps** |
| 15 | IGC_RATE_EN_P0 | **EXP: ingress_rate_limit_exp**<br>MAN: ingress_rate_limit_man<br>The rate of tokens to be filled into token bucket used for ingress rate control: (MAN*10^(EXP)) Kbps<br>0: Ingress rate limit control disable<br>1: Ingress rate limit control Enable |
| 12 | IGC_RATE_CIR_16_P0 | **Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value** |
| 11:8 | IGC_RATE_EXP_P0_IGC_TB_T_P0 | **Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),**<br>When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement,<br>0: 1/128ms<br>1: 1/64ms<br>2: 1/32ms<br>3: 1/16ms<br>4: 1/8ms<br>5: 1/4ms<br>6: 1/2ms<br>7: 1ms<br>8: 2ms<br>9: 4ms<br>10: 8ms<br>11: 16ms<br>12: 32ms<br>13: 64ms<br>14: 128ms<br>15: 128ms |
| 7 | IGC_TB_EN_P0 | **When this bit is disabled, the Ingress rate control acts like a leaky bucket principle.**<br>Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.<br>0: CIR/CBS mode token bucket Disable<br>1: Token bucket mode Enable |
| 6:0 | IGC_RATE_MAN_P0_IGC_TB_CBS_P0 | **Mantissa part of port 0 ingress rate limit control Value range: 0..127 (7-bit),**<br>when IGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and<br>Token Bucket = Max ( IGC_CIR*IGC_TB_T, IGC_TB_CBS*512 ) |

## 2.9 Link Status

You can find MAC control register put at 0x3500 for MAC 5, and 0x3600 for MAC 6. You can change MAC ability at this register. We would suggest don't use the register 0x3000 to 0x3400. It may not work.




**00003500** **PMCR_P5** **PORT 5 MAC Control Register** **00056330**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | IPG_CFG_P5 | | EXT_PHY_P5 | MAC_MODE_P5 |
| Type | | | | | | | | | | | | | RW | | RW | RW |
| Reset | | | | | | | | | | | | | 0 | 1 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FORCE_MODE_P5 | MAC_TX_EN_P5 | MAC_RX_EN_P5 | | MAC_PRE_P5 | | BKOFF_EN_P5 | BACKPR_EN_P5 | FORCE_EEE1G_P5 | FORCE_EEE100_P5 | FORCE_RX_FC_P5 | FORCE_TX_FC_P5 | FORCE_SPD_P5 | | FORCE_DPX_P5 | FORCE_LNK_P5 |
| Type | RW | RW | RW | | RW | | RW | RW | RW | RW | RW | RW | RW | | RW | RW |
| Reset | 0 | 1 | 1 | | 0 | | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 19:18 | IPG_CFG_P5 | **PORT 5 Inter-Frame+ Gap Shrink**<br>00: Normal 96-bits IFG<br>01: Transmit 96-bits IFG with short IFG in random behavior<br>10: Shrink 64-bits IFG |
| 17 | EXT_PHY_P5 | **PORT 5 External PHY**<br>Port 5 connects with external PHY.<br>0: PORT 5 DOES NOT connect with external PHY.<br>1: PORT 5 connects with external PHY. |
| 16 | MAC_MODE_P5 | **PORT 5 MAC Mode**<br>PORT 5 operates in MAC mode.<br>0: PORT 5 operates in PHY mode.<br>1: PORT 5 operates in MAC mode. |
| 15 | FORCE_MODE_P5 | **PORT 5 Force Mode**<br>PORT 5 operates in force mode. It is used to control PORT 5 status of link, speed, duplex, rx_fc, tx_fc, eee100, and eee1g.<br>0: Force mode is off (mac status is determined by phy auto-polling module).<br>1: Force mode is on (mac status is determined by force_xxx_P5 register). |
| 14 | MAC_TX_EN_P5 | **Port 5 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)** |

| | | |
|---|---|---|
| | | 0: TX MAC function is disabled.<br>1: TX MAC function is enabled. |
| 13 | MAC_RX_EN_P5 | **PORT 5 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.)**<br>0: RX MAC function is disabled.<br>1: RX MAC function is enabled. |
| 11 | MAC_PRE_P5 | **TX short preamble mode**<br>0: TX short preamble length is disabled.<br>1: TX short preamble is enabled. |
| 9 | BKOFF_EN_P5 | **PORT 5 Backoff Enable**<br>0: Disabled<br>1: Let the MAC of PORT 5 follow the back-off mechanism when collision happens. |
| 8 | BACKPR_EN_P5 | **PORT 5 Backpressure Enable**<br>0: Disabled<br>1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count. |
| 7 | FORCE_EEE1G_P5 | **PORT 5 Force LPI Mode For 1000Mbps**<br>When (force_mode_P5 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 5.<br>0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps<br>1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps |
| 6 | FORCE_EEE100_P5 | **PORT 5 Force LPI Mode For 100Mbps**<br>When (force_mode_P5 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 5.<br>0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps<br>1: Have the ability of entering EEE Low Power Idle mode for 100Mbps |
| 5 | FORCE_RX_FC_P5 | **PORT 5 Force RX FC**<br>When (force_mode_P5 = 1), this bit is used to control the RX FC ability of PORT 5.<br>0: Disabled.<br>1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode. |
| 4 | FORCE_TX_FC_P5 | **PORT 5 Force TX FC**<br>When (force_mode_P5 = 1), this bit is used to control the TX FC ability of PORT 5.<br>0: Disabled.<br>1: Let the MAC of PORT 5 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2 | FORCE_SPD_P5 | **PORT 5 Force Speed [1:0]**<br>When (force_mode_P5 = 1), these bits are used to control MAC speed of PORT 5.<br>00: 10Mbps<br>01: 100Mbps<br>10: 1000Mbps<br>11: Reserved |
| 1 | FORCE_DPX_P5 | **PORT 5 Force duplex**<br>When (force_mode_P5 = 1), this bit is used to control MAC duplex of PORT 5.<br>0: Half Duplex<br>1: Full Duplex |
| 0 | FORCE_LNK_P5 | **PORT 5 Force MAC Link Up**<br>When (force_mode_P5 = 1), this bit is used to control link status of PORT 5.<br>0: Link Down<br>1: Link Up |

For MAC 5 and MAC6, they have its own status to check register. 0x3508 is for MAC 5 status and 0x3608 is for MAC 6. If you want to change MAC 5 status, you can use 0x3500 to change its ability.

**00003508 PMSR_P5 PORT 5 MAC Status Register 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |

| Type | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | | | | | | EEE1G_STS_P5 | EEE100_STS_P5 | RX_FC_STS_P5 | TX_FC_STS_P5 | MAC_SPD_STS_P5 | | MAC_DPX_STS_P5 | MAC_LNK_STS_P5 |
| Type | | | | | | | | | RO | RO | RO | RO | RO | | RO | RO |
| Reset | | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 7 | EEE1G_STS_P5 | **PORT 5 LPI Mode Status For 1000Mbps**<br>0: Not capable of entering EEE Low Power Idle mode for 1000Mbps<br>1: Capable of entering EEE Low Power Idle mode for 1000Mbps |
| 6 | EEE100_STS_P5 | **PORT 5 LPI Status Mode For 100Mbps**<br>0: Not capable of entering EEE Low Power Idle mode for 100Mbps<br>1: Capable of entering EEE Low Power Idle mode for 100Mbps |
| 5 | RX_FC_STS_P5 | **PORT 5 RX XFC Status. Port 5 Rx flow control status**<br>0: Disabled.<br>1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode. |
| 4 | TX_FC_STS_P5 | **PORT 5 TX XFC Status**<br>PORT 5 TX flow control status<br>0: Disabled.<br>1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count. |
| 3:2 | MAC_SPD_STS_P5 | **PORT 5 Speed [1:0] Status**<br>Current speed of PORT 5 after PHY links up.<br>00: 10 Mbps<br>01: 100 Mbps<br>10: 1000 Mbps<br>11: Reserved |
| 1 | MAC_DPX_STS_P5 | **PORT 5 duplex Status**<br>Current duplex mode of port 5 after PHY links up<br>0: Half Duplex<br>1: Full Duplex |
| 0 | MAC_LNK_STS_P5 | **Port 5 Link Up Status. Link up status of PORT 5.**<br>0: Link Down<br>1: Link Up |

## 2.10 Link Status change

You can find the 0x700c is a record if PHY status was changed. For example, if you plug into PHY 1, you can find the 0x700c become 00080002. Then drew the PHY 1, the 0x700c would still keep 00080002.You need to write “1” to the bit which you want clean at the register 0x700c. After that you can find it would become 00080000.

**0000700C** **SYS_INT_STS** **System Interrupt Status** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | ACL_INT | ARL_SEC_TAG_INT | ARL_SEC_VLAN_INT | ARL_SEC_IG1X_INT | ARL_PKT_BC_INT | ARL_EQ_ERR_INT | ARL_PKT_QERR_INT | ARL_TBL_ERR_INT | | | | | PTP_INT | MIB_INT | BMU_INT | MAC_PC_INT |

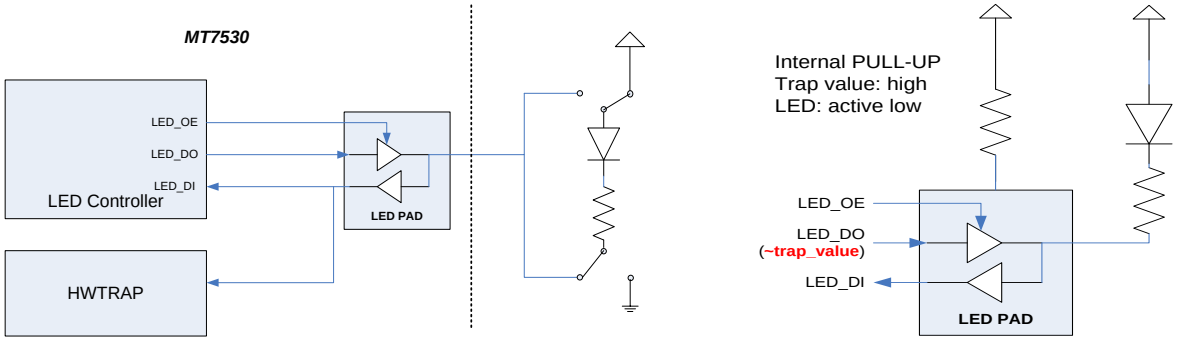
| Type | W1C | W1C | W1C | W1C | W1C | W1C | W1C | W1C | | | | | W1C | W1C | W1C | W1C |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | | | | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | PHY6_INT | PHY5_INT | PHY4_INT | PHY3_INT | PHY2_INT | PHY1_INT | PHY0_INT | | PHY6_LC_INT | PHY5_LC_INT | PHY4_LC_INT | PHY3_LC_INT | PHY2_LC_INT | PHY1_LC_INT | PHY0_LC_INT |
| Type | | W1C | W1C | W1C | W1C | W1C | W1C | W1C | | W1C | W1C | W1C | W1C | W1C | W1C | W1C |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 2.11 LED controller

All hardware traps of GSW are weakly pull-up internally. The only way to pull-down these traps is using an external pull-down circuit. However, hardware traps and LEDs share the same pins in GSW. To make LEDs work normally, the hardware configurations of LEDs will depend on its related values in the current design.
Every port has 1 LED to mean its behavior:

GSW Px_LED_0 is used for any ability linkup and traffic (10/100/1000).

For trapping-high pins, the external LEDs should be active low. Its configuration is shown as below. OEs (output enables) of LED pads are controlled by the internal circuits, and LED_DO will always be LOW under this configuration. So the external LEDs should be active low.




For LED configuration, you can follow the below descrition.

**00007D00 LED_EN LED I/O function enable 00077777**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | P4_LED_EN | | |
| Type | | | | | | | | | | | | | | RW | | |
| Reset | | | | | | | | | | | | | | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | P3_LED_EN | | | | P2_LED_EN | | | | P1_LED_EN | | | | P0_LED_EN | | |
| Type | | RW | | | | RW | | | | RW | | | | RW | | |
| Reset | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 18:16 | P4_LED_EN | **P4 LED I/O Enable**<br>P4_LED_EN[2] for P4 LED #2 |

| | | |
|---|---|---|
| | | P4_LED_EN[1] for P4 LED #1<br>P4_LED_EN[0] for P4 LED #0<br>For individual LED<br>1'b0: Disable<br>1'b1: Enable |
| 14:12 | P3_LED_EN | **P3 LED I/O Enable**<br>P3_LED_EN[2] for P3 LED #2<br>P3_LED_EN[1] for P3 LED #1<br>P3_LED_EN[0] for P3 LED #0<br>For individual LED<br>1'b0: Disable<br>1'b1: Enable |
| 10:8 | P2_LED_EN | **P2 LED I/O Enable**<br>P2_LED_EN[2] for P2 LED #2<br>P2_LED_EN[1] for P2 LED #1<br>P2_LED_EN[0] for P2 LED #0<br>For individual LED<br>1'b0: Disable<br>1'b1: Enable |
| 6:4 | P1_LED_EN | **P1 LED I/O Enable**<br>P1_LED_EN[2] for P1 LED #2<br>P1_LED_EN[1] for P1 LED #1<br>P1_LED_EN[0] for P1 LED #0<br>For individual LED<br>1'b0: Disable<br>1'b1: Enable |
| 2:0 | P0_LED_EN | **P0 LED I/O Enable**<br>P0_LED_EN[2] for P0 LED #2<br>P0_LED_EN[1] for P0 LED #1<br>P0_LED_EN[0] for P0 LED #0<br>For individual LED<br>1'b0: Disable<br>1'b1: Enable |

**00007D04 LED_IO_MODE LED I/O Mode 00077777**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | P4_LED_MODE | | |
| Type | | | | | | | | | | | | | | RW | | |
| Reset | | | | | | | | | | | | | | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | P3_LED_MODE | | | | P2_LED_MODE | | | | P1_LED_MODE | | | | P0_LED_MODE | | |
| Type | | RW | | | | RW | | | | RW | | | | RW | | |
| Reset | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 | | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 18:16 | P4_LED_MODE | **P4 LED I/O Mode**<br>P4_LED_MODE[2] for P4 LED #2<br>P4_LED_MODE[1] for P4 LED #1<br>P4_LED_MODE[0] for P4 LED #0<br>For individual LED Mode<br>1'b0: GPIO<br>1'b1: LED |
| 14:12 | P3_LED_MODE | **P3 LED I/O Mode**<br>P3_LED_MODE[2] for P3 LED #2<br>P3_LED_MODE[1] for P3 LED #1<br>P3_LED_MODE[0] for P3 LED #0<br>For individual LED Mode<br>1'b0: GPIO<br>1'b1: LED |

| | | |
|---|---|---|
| 10:8 | P2_LED_MODE | **P2 LED I/O Mode**<br>P2_LED_MODE[2] for P2 LED #2<br>P2_LED_MODE[1] for P2 LED #1<br>P2_LED_MODE[0] for P2 LED #0<br>For individual LED Mode<br>1'b0: GPIO<br>1'b1: LED |
| 6:4 | P1_LED_MODE | **P1 LED I/O Mode**<br>P1_LED_MODE[2] for P1 LED #2<br>P1_LED_MODE[1] for P1 LED #1<br>P1_LED_MODE[0] for P1 LED #0<br>For individual LED Mode<br>1'b0: GPIO<br>1'b1: LED |
| 2:0 | P0_LED_MODE | **P0 LED I/O Mode**<br>P0_LED_MODE[2] for P0 LED #2<br>P0_LED_MODE[1] for P0 LED #1<br>P0_LED_MODE[0] for P0 LED #0<br>For individual LED Mode<br>1'b0: GPIO<br>1'b1: LED |

If you want to change the LED behavior, please write these registers of Ethernet physical.

**51F00240 dev1Fh_reg024h LED0 On Control Register 8000**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | rg_led0_en | rg_led0_pol | | | | | | | | led0_on_mask | | | | | | |
| Type | RW | RW | | | | | | | | RW | | | | | | |
| Reset | 1 | 0 | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15 | rg_led0_en | **Enable Ethernet LED Function.**<br>0: Disable (Hi-Z)<br><br>1: Enable |
| 14 | rg_led0_pol | **Select LED polarity. This field only takes effect when LED_EN is 1b1.**<br>Enable Ethernet LED Function.<br>0: Active low (That is, LED On means Output 0)<br><br>1: Active high (That is, LED On means Output 1) |
| 6:0 | led0_on_mask | **LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.**<br>Select LED polarity. This field only takes effect when LED_EN is 1b1.<br>Bit[0]:Link 1000<br>Bit[1]:Link 100<br>Bit[2]:Link 10<br>Bit[3]:Link Down<br>Bit[4]:Full Duplex<br>Bit[5]:Half Duplex<br>Bit[6]:Force On (Logic 1) |

**51F00250 dev1Fh_reg025h LED0 Blinking Control Register 0000**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | led0_blk_mask | | | | | | | | | |
| Type | | | | | | | RW | | | | | | | | | |

| Reset | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Bit(s) | Name | Description |
|---|---|---|
| 9:0 | led0_blk_mask | **LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.**<br>(Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is)<br>Bit[0]:1000Mbps TX Activity<br>Bit[1]:1000Mbps RX Activity<br>Bit[2]:100Mbps TX Activity<br>Bit[3]:100Mbps RX Activity<br>Bit[4]:10Mbps TX Activity<br>Bit[5]:10Mbps RX Activity<br>Bit[6]:Collision<br>Bit[7]:RX CRC Error<br>Bit[8]:RX Idle Error<br>Bit[9]:Force Blinks (Logic 1) |

## 51F00260 dev1Fh_reg026h LED1 On Control Register 8000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | rg_led1_en | rg_led1_pol | | | | | | | | led1_on_mask | | | | | | |
| Type | RW | RW | | | | | | | | RW | | | | | | |
| Reset | 1 | 0 | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15 | rg_led1_en | **Enable Ethernet LED Function.**<br>0: Disable (Hi-Z)<br><br>1: Enable |
| 14 | rg_led1_pol | **Select LED polarity. This field only takes effect when LED_EN is 1b1.**<br>Enable Ethernet LED Function.<br>0: Active low (That is, LED On means Output 0)<br><br>1: Active high (That is, LED On means Output 1) |
| 6:0 | led1_on_mask | **LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.**<br>Select LED polarity. This field only takes effect when LED_EN is 1b1.<br>Bit[0]:Link 1000<br>Bit[1]:Link 100<br>Bit[2]:Link 10<br>Bit[3]:Link Down<br>Bit[4]:Full Duplex<br>Bit[5]:Half Duplex<br>Bit[6]:Force On (Logic 1) |

## 51F00270 dev1Fh_reg027h LED1 Blinking Control Register 0000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | led1_blk_mask | | | | | | | | | |
| Type | | | | | | | RW | | | | | | | | | |
| Reset | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 9:0 | led1_blk_mask | **LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.** |

(Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter LED-On status is)
Bit[0]:1000Mbps TX Activity
Bit[1]:1000Mbps RX Activity
Bit[2]:100Mbps TX Activity
Bit[3]:100Mbps RX Activity
Bit[4]:10Mbps TX Activity
Bit[5]:10Mbps RX Activity
Bit[6]:Collision
Bit[7]:RX CRC Error
Bit[8]:RX Idle Error
Bit[9]:Force Blinks (Logic 1)

## 51F00280 dev1Fh_reg028h LED2 On Control Register 8000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | rg_led2_en | rg_led2_pol | | | | | | | | led2_on_mask | | | | | | |
| Type | RW | RW | | | | | | | | RW | | | | | | |
| Reset | 1 | 0 | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15 | rg_led2_en | **Enable Ethernet LED Function.**<br>0: Disable (Hi-Z)<br><br>1: Enable |
| 14 | rg_led2_pol | **Select LED polarity. This field only takes effect when LED_EN is 1b1.**<br>Enable Ethernet LED Function.<br>0: Active low (That is, LED On means Output 0)<br><br>1: Active high (That is, LED On means Output 1) |
| 6:0 | led2_on_mask | **LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.**<br>Select LED polarity. This field only takes effect when LED_EN is 1b1.<br>Bit[0]:Link 1000<br>Bit[1]:Link 100<br>Bit[2]:Link 10<br>Bit[3]:Link Down<br>Bit[4]:Full Duplex<br>Bit[5]:Half Duplex<br>Bit[6]:Force On (Logic 1) |

## 51F00290 dev1Fh_reg029h LED2 Blinking Control Register 0000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | led2_blk_mask | | | | | | | | | |
| Type | | | | | | | RW | | | | | | | | | |
| Reset | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 9:0 | led2_blk_mask | **LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.**<br>(Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is)<br>Bit[0]:1000Mbps TX Activity<br>Bit[1]:1000Mbps RX Activity<br>Bit[2]:100Mbps TX Activity<br>Bit[3]:100Mbps RX Activity<br>Bit[4]:10Mbps TX Activity |

Bit[5]:10Mbps RX Activity
Bit[6]:Collision
Bit[7]:RX CRC Error
Bit[8]:RX Idle Error
Bit[9]:Force Blinks (Logic 1)

### 51F002A0 dev1Fh_reg02Ah LED3 On Control Register 8000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | rg_led3_en | rg_led3_pol | | | | | | | | led3_on_mask | | | | | | |
| Type | RW | RW | | | | | | | | RW | | | | | | |
| Reset | 1 | 0 | | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15 | rg_led3_en | **Enable Ethernet LED Function.**<br>0: Disable (Hi-Z)<br><br>1: Enable |
| 14 | rg_led3_pol | **Select LED polarity. This field only takes effect when LED_EN is 1b1.**<br>Enable Ethernet LED Function.<br>0: Active low (That is, LED On means Output 0)<br><br>1: Active high (That is, LED On means Output 1) |
| 6:0 | led3_on_mask | **LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1.**<br>Select LED polarity. This field only takes effect when LED_EN is 1b1.<br>Bit[0]:Link 1000<br>Bit[1]:Link 100<br>Bit[2]:Link 10<br>Bit[3]:Link Down<br>Bit[4]:Full Duplex<br>Bit[5]:Half Duplex<br>Bit[6]:Force On (Logic 1) |

### 51F002B0 dev1Fh_reg02Bh LED3 Blinking Control Register 0000

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | led3_blk_mask | | | | | | | | | |
| Type | | | | | | | RW | | | | | | | | | |
| Reset | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 9:0 | led3_blk_mask | **LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1.**<br>(Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is)<br>Bit[0]:1000Mbps TX Activity<br>Bit[1]:1000Mbps RX Activity<br>Bit[2]:100Mbps TX Activity<br>Bit[3]:100Mbps RX Activity<br>Bit[4]:10Mbps TX Activity<br>Bit[5]:10Mbps RX Activity<br>Bit[6]:Collision<br>Bit[7]:RX CRC Error<br>Bit[8]:RX Idle Error<br>Bit[9]:Force Blinks (Logic 1) |

## 2.12 Loop Detection

When loop detection function is enabled by setting hardware strapping(0x7804), the GSW provide two different signal out. One is sent the loop frame with the SID as 0180c2000001, another is sent the period LED.
Follow the step to check it:

1. Set 0x30c0 ( for example : enable p0,p1,p3, set as 0x07130000)
2. Set 0x201c,0x211c ..0x261c to enable per port broadcast storm detection( for example, set 0x201c as cc030303 for port 0)

   After that, you can check the Loop frame and alarm signal from 96th pin.

3. Read 0x30c0 to check the Alarm message.
   (You can write bit 1 of 0x30c0 as 1 to clean the status)

**000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00030000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | LPDET_EN6 | LPDET_EN5 | LPDET_EN4 | LPDET_EN3 | LPDET_EN2 | LPDET_EN1 | LPDET_EN0 | LPDET_PERIOD_EN | LPDET_ALARM_EN | LPDET_PASS | LPDET_PERIOD | LPDET_LED_RATE | LPDET_THRESHOLD | | |
| Type | | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | | |
| Reset | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | LPDET_ST_LOOP | LPDET_ST_BCST | LPDET_TRAP_EN | | | | | | | LPDET_ALARM6 | LPDET_ALARM5 | LPDET_ALARM4 | LPDET_ALARM3 | LPDET_ALARM2 | LPDET_ALARM1 | LPDET_ALARM0 |
| Type | RO | RO | RO | | | | | | | RO | RO | RO | RO | RO | RO | W1C |
| Reset | 0 | 0 | 0 | | | | | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 30 | LPDET_EN6 | **Enable the loop detection ability of user port 6.**<br>0: Disable<br>1: Enable |
| 29 | LPDET_EN5 | **Enable loop detection the ability of user port 5.**<br>0: Disable<br>1: Enable |
| 28 | LPDET_EN4 | **Enable loop detection the ability of user port 4.**<br>0: Disable<br>1: Enable |
| 27 | LPDET_EN3 | **Enable loop detection the ability of user port 3.**<br>0: Disable<br>1: Enable |
| 26 | LPDET_EN2 | **Enable loop detection the ability of user port 2.**<br>0: Disable<br>1: Enable |
| 25 | LPDET_EN1 | **Enable loop detection the ability of user port 1.**<br>0: Disable<br>1: Enable |
| 24 | LPDET_EN0 | **Enable loop detection the ability of user port 0.** |

| | | |
|---|---|---|
| | | 0: Disable<br>1: Enable |
| 23 | LPDET_PERIOD_EN | **The loop detection frame is triggered by a periodical timer or by broadcast storm.**<br>0: Broadcast mode<br>1: Periodical mode |
| 22 | LPDET_ALARM_EN | **Enable 2 kHz alarm output and per-port LED when loop is detected.**<br>0: Disable<br>1: Enable |
| 21 | LPDET_PASS | **Loop detection frame is blocked or passed to packet memory.**<br>0: Blocked<br>1: Pass |
| 20 | LPDET_PERIOD | **Interval of transmitting loop detection frame in Periodical mode.**<br>0: 125 us<br>1: 1000 ms |
| 19 | LPDET_LED_RATE | **LED blinking rate of per port when loop is detected.**<br>0: LED blinking at 2 Hz<br>1: LED blinking at 4 Hz |
| 18:16 | LPDET_THRESHOLD | **Number of missed loop detection frame before 2 kHz alarm is reset** |
| 15 | LPDET_ST_LOOP | **The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received.**<br>0: Not in Loop state<br>1: Loop state |
| 14 | LPDET_ST_BCST | **The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received.**<br>0: Not in BCST state<br>1: BCST state |
| 13 | LPDET_TRAP_EN | **Status of strap pin for loop detection**<br>0: Disabled<br>1: Enabled |
| 6 | LPDET_ALARM6 | **The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 5 | LPDET_ALARM5 | **The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 4 | LPDET_ALARM4 | **The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 3 | LPDET_ALARM3 | **The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 2 | LPDET_ALARM2 | **The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 1 | LPDET_ALARM1 | **The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1.**<br>0: Not detected<br>1: Detected |
| 0 | LPDET_ALARM0 | **The status of loop detected on port 0. This bit is cleared when it is written as 1.**<br>0: Not detected<br>1: Detected |

**0000201C** **BSR** **Broadcast Storm Rate Control of P0** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | STRM_MODE | STRM_BC_INC | STRM_MC_INC | STRM_UC_INC | STRM_DROP | STRM_PERD | STRM_UNIT | | STORM_1G | | | | | | | |
| Type | RW | RW | RW | RW | RW | RW | RW | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | STORM_100M | | | | | | | | STORM_10M | | | | | | | |
| Type | RW | | | | | | | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | STRM_MODE | **Broadcast Storm Suppression**<br>0: Packet-based ( 1 second period)<br>1: Rate-based |
| 30 | STRM_BC_INC | **Broadcast Storm Included**<br>0: Exclude BC frame<br>1: Include BC frame |
| 29 | STRM_MC_INC | **Unknown Multicast Storm Included**<br>0: Exclude MC frame<br>1: Include MC frame |
| 28 | STRM_UC_INC | **Unknown Unicast Storm Included**<br>0: Exclude UC frame<br>1: Include UC frame |
| 27 | STRM_DROP | **Broadcast Storm Suppression enabled**<br>0: BC Storm detection only<br>1: Enable packet drop when BC storm is detected |
| 26 | STRM_PERD | **Broadcast Strom Detection Signal Period**<br>0: One second<br>1: 125us |
| 25:24 | STRM_UNIT | **Broadcast Storm Suppression**<br>2'b00: 64 packets or 64 Kbps<br>2'b01: 256 packets or 256 Kbps<br>2'b10: 1 K packets or 1 Mbps<br>2'b11: 4 K packets or 4 Mbps |
| 23:16 | STORM_1G | **1000 Mbps Broadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 1000 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |
| 15:8 | STORM_100M | **100 Mbps Broadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 100 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bp |
| 7:0 | STORM_10M | **10 MbpsBroadcast Storm Rate Limit Control**<br>The broadcast storm rate limit for 10 Mbps link speed<br>8'h0: (0* STORM_UNIT) packets or bps<br>8'h1: (1* STORM_UNIT) packets or bps |

## 2.13 MAC forward control

0x0010 is used for MAC forwarding control rule. For different traffic, like broadcast, Unknown multicast...etc, you can set the forwarding port at this register.

**00000010 MFC MAC Forward Control 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | BC_FFP | | | | | | | | UNM_FFP | | | | | | | |
| Type | RW | | | | | | | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | UNU_FFP | | | | | | | | CPU_EN | CPU_PORT | | | MIRROR_EN | MIRROR_PORT | | |
| Type | RW | | | | | | | | RW | RW | | | RW | RW | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:24 | BC_FFP | **Broadcast Frame Flooding Ports**<br>If MAC receives broadcast frames, this field indicates the flooding ports.<br>[NOTE]<br>1. The flooding port excludes the received port on the switch.<br>2. Frame dropped though BC_FFP=6'b0 |
| 23:16 | UNM_FFP | **Unknown Multicast Frame Flooding Ports**<br>If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports.<br>[NOTE]<br>1. The flooding port will exclude the received port by HW.<br>2. Frame dropped though UNM_FFP=6'b0. |
| 15:8 | UNU_FFP | **Unknown Unicast Frame Flooding Ports**<br>If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port.<br>[NOTE]<br>1. The flooding port will excludes the received port by HW<br>2. Frame dropped though UNM_FFP=6'b0 |
| 7 | CPU_EN | **CPU Port Enable**<br>Enable the CPU port specified in CPU_PORT.<br>0: No CPU port exists.<br>1: Enable |
| 6:4 | CPU_PORT | **CPU Port Number**<br>Set the CPU port number.<br>3'h0: Port 0<br>...<br>3'h7: Port 7 |
| 3 | MIRROR_EN | **Mirror Port Enable**<br>Enable the mirror port specified in MIRROR_PORT.<br>0: No mirror available<br>1: Enable mirror |
| 2:0 | MIRROR_PORT | **Mirror Port Number**<br>Set the mirror port number.<br>3'h0: Port 0<br>...<br>3'h7: Port 7 |

Here also show the forwarding rule which you can set at register 0x0010.

| FTAG | ACL Enable | ARL/DIP Table | Action |
|---|---|---|---|

| | | | |
|---|---|---|---|
| BC | ACL Hit and Port Map is enabled | - | Follow ACL Forwarding Port Map |
| | Disable or ACL not Hit | - | Follow MFC .BC_FFP register |
| MC<br>IP_MULT<br>IPV6_MULTI | ACL Hit and Port Map is enabled | - | Follow ACL Forwarding Port Map |
| | Disable or ACL not Hit | ARL Hit | Follow ARL Forwarding Port Map |
| | | ARL not Hit | Follow MFC.UNM_FFP register |
| UC | ACL Hit and Port Map is enabled | - | Follow ACL Forwarding Port Map |
| | Disable or ACL not Hit | ARL Hit | Follow ARL Forwarding Port Map |
| | | ARL not Hit | Follow MFC.UNU_FFP register |

## 2.14MAC table aging time

Aging time is used for recording the MAC is exist or not and would be clean after 300 seconds if there is no traffic pass through again. For changing this, you can modify the 0x00A0.

The aging time would be depending on the switch core clock speed.

**000000A0 AAC Address Age Control 00095001**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | | | | | | | | | | | AGE_DIS | AGE_CNT[7:4] | | | |
| Type | DC | | | | | | | | | | | RW | RW | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | AGE_CNT[3:0] | | | | AGE_UNIT | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:21 | REV0 | **Reserved** |
| 20 | AGE_DIS | **Address Table Aging Disable**<br>Disable or pause MAC address aging. |
| 19:12 | AGE_CNT | **Address Table Age Count**<br>This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds. |
| 11:0 | AGE_UNIT | **Address Table Age Unit**<br>The applied aging unit is equal to (AGE_UNIT+1) seconds. |

## 2.15 MAC table

We have 2048 MAC entries exist in switch.
GSW build in the API command:
Ethphxcmd arl mactbl-disp
MAC AABBCCDDEEFF : TIMER:149, SA_PORT_FW:0, SA_MIR_EN:0, USER_PRI:0, EG_TAG:0, LEAKY_EN:0, PORT:4, STATUS:1, TYPE:0
You can find that have an aging time, source port information over there.

For RT63368 or others platform, you can use the command flow to check the MAC table list:

```
Ethphxcmd gsww 80 8002   //clean
Ethphxcmd gsww 80 8004   //first MAC entry
Ethphxcmd gswr 84        // show the first entry
Ethphxcmd gswr 88        // show the firstentry
Ethphxcmd gsww 80 8005   //next MAC entry
Ethphxcmd gswr 84        // show the second entry
Ethphxcmd gswr 88        // show the second entry
```

For detail, you can check the register 0x0080,0x0084 and 0x0088.

**00000080 ATC Address Table Control 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | | | | ADDR | | | | | | | | | | | |
| Type | DC | | | | RO | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | BUSY | SRCH_END | SRCH_HIT | ADDR_INVLD | AC_MAT | | | | REV1 | | AC_SAT | | REV2 | AC_CMD | | |
| Type | W1C | RO | RO | RO | RW | | | | DC | | RW | | DC | RW | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**00000084 TSRA1 Table Search Read Address I 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | BYTE_0 | | | | | | | | BYTE_1 | | | | | | | |
| Type | RO | | | | | | | | RO | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | BYTE_2 | | | | | | | | BYTE_3 | | | | | | | |
| Type | RO | | | | | | | | RO | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:24 | BYTE_0 | **MAC Address[47:40] / Destination IP(DIP) Address [31:24]** |
| 23:16 | BYTE_1 | **MAC Address[39:32] / Destination IP(DIP) Address [23:16]** |
| 15:8 | BYTE_2 | **MAC Address[31:24] / Destination IP(DIP) Address [15:8]** |
| 7:0 | BYTE_3 | **MAC Address[23:16] / Destination IP(DIP) Address [7:0]** |

**00000088 TSRA2 Table Search Read Address II 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | BYTE_0 | | | | | | | | BYTE_1 | | | | | | | |
| Type | RO | | | | | | | | RO | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | BYTE_2 | | | | | | | | BYTE_3 | | | | | | | |
| Type | RO | | | | | | | | RO | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:24 | BYTE_0 | **MAC Address[15:8] / Source IP(SIP) Address [31:24]** |
| 23:16 | BYTE_1 | **MAC Address[7:0] / Source IP(SIP) Address [23:16]** |
| 15:8 | BYTE_2 | **SIP Address [15: 8] or**<br>bit[15]: IVL<br>bit[14:12]: Filter ID[2:0]<br>bit[11:8]: CVID[11: 8]<br>NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table. |
| 7:0 | BYTE_3 | **SIP Address[7:0] or CVID[7:0]** |

## 2.16 Output queue

Each port has 8 queues for different QoS services. Please know that QoS only active when traffic jam happen. It means that you should have flow control first for QoS. If not, you would only find the packet loss.
Free page: Read the 0x1fc0

For GSW, if you want to check the queue, please use:
ethphxcmd gsww 7038 220
ethphxcmd gswr 7034

Here show the Q map:

| | Q1 & Q0 | Q3 & Q2 | Q5 & Q4 | Q7 & Q6 |
|---|---|---|---|---|
| P0 | 220 | 221 | 222 | 223 |
| P1 | 224 | 225 | 226 | 227 |
| P2 | 228 | 229 | 22a | 22b |
| P3 | 22c | 22d | 22e | 22f |
| P4 | 230 | 231 | 232 | 233 |
| P5 | 234 | 235 | 236 | 237 |
| P6 | 238 | 239 | 23a | 23b |

**00001FC0 FPLC Free Page Link Count Register 01EE01EE**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

| Name | | | | | | | MIN_FREE_PL_CNT | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | | | | | | | RO | | | | | | | | | |
| Reset | | | | | | | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | | | | | | | FREE_PL_CNT | | | | | | | | | |
| Type | | | | | | | RO | | | | | | | | | |
| Reset | | | | | | | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 25:16 | MIN_FREE_PL_CNT | **Minimal Free Page Link Count in LMU from last read access** |
| 9:0 | FREE_PL_CNT | **Free Page Link Count in LMU** |

## 2.17VLAN setting

You need use three registers to make one VLAN rule. Please follow the below information to do that:
Set the port you want into security mode and as user port, take port 1 as example:

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port
You should set up the each VLAN port you want to be security mode and user port.
Next, you need to setup the VLAN ID and group member. Here, we set port 0 to 3 and port 6 as one group and their VLAN ID is 10. And just only port 3 get the egress tag.

0x94 104F0001 Port member 0~3+6 (4f =0100 1111 )
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98
0x90 80001003 VID member VID set as 03
Note: Please don't use 0 and 4095 for VID.

If you do not want to add egress tag at any port, just set 0x98 as 0. For detail, check the register 0x0098 at the below.

**00002104** **PCR** **Port Control of P1** **00FF0000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | MLDv2_EN | EG_TAG | | REV1 | PORT_PRI | | | PORT_MATRIX | | | | | | | |
| Type | DC | RW | RW | | DC | RW | | | RW | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | REV2 | | | UP2DSCP_EN | UP2TAG_EN | ACL_EN | PORT_TX_MIR | PORT_RX_MIR | ACL_MIR | MIS_PORT_FW | | | REV3 | VLAN_MIS | PORT_VLAN | |
| Type | DC | | | RW | RW | RW | RW | RW | RW | RW | | | DC | RW | RW | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## 00000090 VTCR VLAN Table Control 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | BUSY | REV0 | | | | | | | | | | | | | | IDX_INVLD |
| Type | W1C | DC | | | | | | | | | | | | | | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | FUNC | | | | VID | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | BUSY | **VLAN Table Is Busy**<br>SW can set this bit to 1 only if this bit is reset. After the VTCR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. |
| 30:17 | REV0 | **Reserved** |
| 16 | IDX_INVLD | **Entry is not Valid**<br>This index for the access control is out of the valid index. |
| 15:12 | FUNC | **Access Control Function**<br>Whenever VTCR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.<br>4'b0000: Read the specified VID Entry from VAWD# register based on VID bits<br>4'b0001: Write the specified VID Entry though VAWD# register based on VID bits.<br>4'b0010: Make the specified VID entry invalid based on VID bits.<br>4'b0011: Make the specified VID entry valid based on VID bits .<br>4'b0100: Read the specified ACL Table entry.<br>4'b0101: Write the specified ACL Table entry.<br>4'b0110: Read the specified trTCM Meter Table.<br>4'b0111: Write the specified trTCM Meter Table.<br>4'b1000: Read the specified ACL Mask entry.<br>4'b1001: Write the specified ACL Mask entry.<br>4'b1010: Read the specified ACL Rule Control entry.<br>4'b1011: Write the specified ACL Rule Control entry.<br>4'b1100: Read the specified ACL Rate Control entry.<br>4'b1101: Write the specified ACL Rate Control entry.<br>4'b1110: Reserved<br>4'b1111: Reserved |
| 11:0 | VID | **1. VLAN ID Number: 0x0 to 0x1F (16)**<br>2. ACL table index: 0x0 to 0x3F (64)<br>3. ACL mask control: 0x0 to 0x3F (32 or 64) |

## 00000094 VAWD1 VLAN and ACL Write Data I 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | WDATA[31:16] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | WDATA[15:0] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(VLAN Entry)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31 | RW | PORT_STAG | Port based STAG | 0x0 |
| 30 | RW | IVL_MAC | Independent VLAN Learning | 0x0 |
| 29 | RW | EG_CON | Egress Tag Consistent | 0x0 |
| 28 | RW | VTAG_EN | Per VLAN Egress Tag Control | 0x0 |
| 27 | RW | COPY_PRI | Copy User Priority Value from Customer Priority Tag for Stack VLAN | 0x0 |
| 26:24 | RW | USER_PRI | Service Tag User Priority Value from VLAN Table | 0x0 |
| 23:16 | RW | PORT_MEM | VLAN Member Control | 0x0 |
| 15:4 | RW | S_TAG1 | Service Tag I | 0x0 |
| 3:1 | RW | FID | Filtering Database | 0x0 |
| 0 | RW | VALID | VLAN Entry Valid | 0x0 |

**00000098 VAWD2 VLAN and ACL Write Data II 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | WDATA[31:16] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | WDATA[15:0] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

(VLAN Entry)

| Bits | Type | Name | Description | Initial value |
|---|---|---|---|---|
| 31:16 | RW | S_TAG2 | Service Tag II | 0x0 |
| 15:14 | - | - | Reserved | 0x0 |
| 13:12 | RW | P6_TAG | P6 Egress Tag Control | 0x0 |
| 11:10 | RW | P5_TAG | P5 Egress Tag Control | 0x0 |
| 9:8 | RW | P4_TAG | P4 Egress Tag Control | 0x0 |
| 7:6 | RW | P3_TAG | P3 Egress Tag Control | 0x0 |
| 5:4 | RW | P2_TAG | P2 Egress Tag Control | 0x0 |
| 3:2 | RW | P1_TAG | P1 Egress Tag Control | 0x0 |
| 1:0 | RW | P0_TAG | P0 Egress Tag Control | 0x0 |

**00002010 PVC Port VLAN Control of P0 000000C0**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | STAG_VPID | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DIS_PVID | FORCE_PVID | REV0 | PT_VPM | PT_OPTION | EG_TAG | | | VLAN_ATTR | | PORT_STAG | BC_LKYV_EN | MC_LKYV_EN | UC_LKYV_EN | ACC_FRM | |
| Type | RW | RW | DC | RW | RW | RW | | | RW | | RW | RW | RW | RW | RW | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

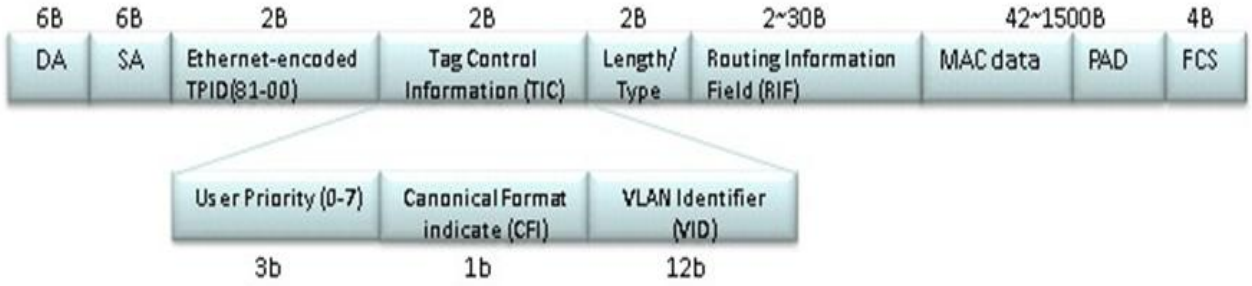
| Bit(s) | Name | Description |
|---|---|---|
| 31:16 | STAG_VPID | **Stack Tag VPID (VLAN Protocol ID) Value**<br>The received frame will be regarded as a legal stack tag frame if the following conditions are matched:<br>Outer VPID == STAG_VPID<br>Inner VPID == 16'h8100<br>The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID. |
| 15 | DIS_PVID | **PVID Disable**<br>Disable PVID insertion in priority-tagged frames.<br>0: Use PVID for priority-tagged frames.<br>1: Keep VID=0 for priority-tagged frames. |
| 14 | FORCE_PVID | **Force PVID on VLAN-tagged frames**<br>0: Use VID in VLAN-tagged frame.<br>1: Force the replacement of VID with PVID . |
| 13 | REV0 | |
| 12 | PT_VPM | **Pass-through capability on TPID**<br>0: Disable pass-through on TPID<br>1: Enable pass-through on TPID |
| 11 | PT_OPTION | **Pass-through capability on TX special tag**<br>0: Disable pass-through on TX special tag<br>1: Enable pass-through on TX special tag |
| 10:8 | EG_TAG | **Incoming Port Egress VLAN Tag Attribution**<br>3'b000: System default (disabled)<br>3'b001: Consistent<br>3'b010, 3'b011: Reserved<br>3'b100: Untagged<br>3'b101: Swap<br>3'b110: Tagged<br>3'b111: Stack |
| 7:6 | VLAN_ATTR | **VLAN Port Attribute**<br>2'b00: User port<br>2'b01: Stack port<br>2'b10: Translation port<br>2'b11: Transparent port |
| 5 | PORT_STAG | **Special Tag Enable**<br>Enable a proprietary VLAN tag format to carry additional information to the remote port.<br>0: No special tag format for Tx/Rx<br>1: Enable |
| 4 | BC_LKYV_EN | **Broadcast Leaky VLAN Enable**<br>0: Broadcast frames received by this port will be blocked by VLAN.<br>1: Broadcast frames received by this port can pass through VLAN. |
| 3 | MC_LKYV_EN | **Multicast Leaky VLAN Enable**<br>[NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.)<br>0: Multicast frames received by this port will be blocked by VLAN. |

| | | |
|---|---|---|
| | | 1: Multicast frames received by this port can pass through VLAN. |
| 2 | UC_LKYV_EN | **Unicast Leaky VLAN Enable**<br>[NOTE] Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MAC.UC_ARL_LKYV or MAC.UC_ARL_LKYV.)<br>0: Unicast frame received by this port will be blocked by VLAN.<br>1: Unicast frame received by this port can pass through VLAN. |
| 1:0 | ACC_FRM | **Acceptable Frame Type**<br>2'b00: Admit All frames<br>2'b01: Admit Only VLAN-tagged frames<br>2'b10: Admit only untagged or priority-tagged frames.<br>2'b11: Reserved |

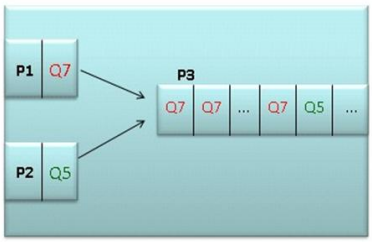
Note: if you want to drop (or not)packet with VLAN tag(or not), you can set bit 1:0 of REG 0x2010,0x2110,0x2210…0x2610 to do that.

## 2.18 QoS (Quality of Services)

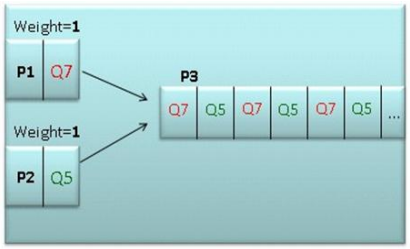
QoS is the ability to provide different priority to different applications or the data flows. GSW can support strict priority (SP) and weighted round-robin (WRR) mode for QoS. Please refer to packet format at the below figure and know the VID and user priority are the key for QoS. We will suggest that you should disable flow control if you want to use QoS.




**SP:**




**WRR:**



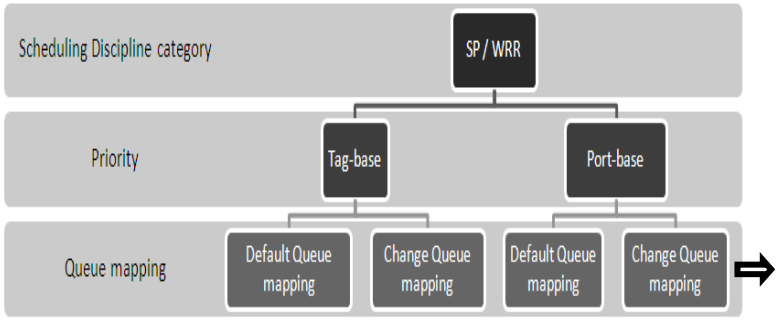

You may need to make the port you want as security mode and user port first. For detail, please check the page about VALN setting in this document.

0x 2104 00ff0003 //set as security mode
0x 2110 81000000 //set as user port

0x94 104F0001 Port member 0~3+6 (4f =0100 1111 )
0x98 000000c0 Egress tag enable for port 3 , refer to register 0x98

0x90 80001003 VID member VID set as 03
Please also refer the chapter of VLAN to know the detail setting.

Follow the step to setup the QoS:




Default Priority-to-queue mapping
(802.3D QoS)
Priority 7 – Queue 7
Priority 6 – Queue 6
Priority 5 – Queue 5
Priority 4 – Queue 4
Priority 3 – Queue 3
Priority 1 – Queue 2
Priority 0 – Queue 1
Priority 2 – Queue 0

You can swap the Q map as you want.
For example:
Change priority 1 from Q2 to Q1:
0x0048 09080240
Change priority 1 from Q1 to Q2:
0x0048 0a080240

Please notice the GSW use output queue structure.
That means you should set these setting at output port.
Set as Tag-base
0x0044 as 0x222722 //Tag-base for first priority

If want to use SP:
0x1000 as 0x80000000 //SP for Q0 of Port 0
0x1004 as 0x00000000 //SP for Q0 of Port 0
0x1008 as 0x80000000 //SP for Q1 of Port 0
0x100c as 0x00000000 //SP for Q1 of Port 0

If want to use WRR:
0x1000 as 0x80008000 //WRR for Q0 of P0
0x1004 as 0x01000000 //weight of Q0 of P0
0x1008 as 0x80008000 //WRR for Q1 of P0
0x100c as 0x03000000 //weight of Q1 of P0

Set the port weight:
0x1004 as 0x01000000 //Weighting of P0 Q0 is 2 ( **q0_max_weight+1'b1)**
0x100c as 0x03000000 //Weighting of P0 Q1 is 4 ( **q1_max_weight+1'b1)**
…
**Note: Queue n service with probability Pn (Pn = weight n / Sum (weight))**

Follow the table and set the mode as SP or WRR.

| | Q0 | Q1 | Q2 | Q3 | Q4 | Q5 | Q6 | Q7 |
|---|---|---|---|---|---|---|---|---|
| Port 0 | 0x1000 | 0x1008 | 0x1010 | 0x1018 | 0x1020 | 0x1028 | 0x1030 | 0x1038 |
| Port 1 | 0x1100 | 0x1108 | 0x1110 | 0x1118 | 0x1120 | 0x1128 | 0x1130 | 0x1138 |
| Port 2 | 0x1200 | 0x1208 | 0x1210 | 0x1218 | 0x1220 | 0x1228 | 0x1230 | 0x1238 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Port 3 | 0x1300 | 0x1308 | 0x1310 | 0x1318 | 0x1320 | 0x1328 | 0x1330 | 0x1338 |
| Port 4 | 0x1400 | 0x1408 | 0x1410 | 0x1418 | 0x1420 | 0x1428 | 0x1430 | 0x1438 |
| Port 5 | 0x1500 | 0x1508 | 0x1510 | 0x1518 | 0x1520 | 0x1528 | 0x1530 | 0x1538 |
| Port 6 | 0x1600 | 0x1608 | 0x1610 | 0x1618 | 0x1620 | 0x1628 | 0x1630 | 0x1638 |

P0 weighting setting map:

| | | | |
|---|---|---|---|
| 00001004 | **MMSCR1_Q0P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 0/Port 0** |
| 0000100C | **MMSCR1_Q1P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 1/Port 0** |
| 00001014 | **MMSCR1_Q2P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 2/Port 0** |
| 0000101C | **MMSCR1_Q3P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 3/Port 0** |
| 00001024 | **MMSCR1_Q4P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 4/Port 0** |
| 0000102C | **MMSCR1_Q5P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 5/Port 0** |
| 00001034 | **MMSCR1_Q6P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 6/Port 0** |
| 0000103C | **MMSCR1_Q7P0** | 32 | **Max-Min Scheduler Control Register 1 of Queue 7/Port 0** |

**00000044 UPW User Priority Weight 00234567**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | | | | | | | | | ARL_UPW | | | REV1 | PORT_UPW | | |
| Type | DC | | | | | | | | | RW | | | DC | RW | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | REV2 | DSCP_UPW | | | REV3 | TAG_UPW | | | REV4 | STAG_UPW | | | REV5 | ACL_UPW | | |
| Type | DC | RW | | | DC | RW | | | DC | RW | | | DC | RW | | |
| Reset | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:23 | REV0 | **Reserved** |
| 22:20 | ARL_UPW | **ARL User Priority Weight (MAC/DIP Hit)** |
| 19 | REV1 | **Reserved** |
| 18:16 | PORT_UPW | **Port-Based User Priority Weight Value**<br>Weights range from 0x0 to 0x7. |
| 15 | REV2 | **Reserved** |
| 14:12 | DSCP_UPW | **DSCP Priority Weight (IPv4)** |
| 11 | REV3 | **Reserved** |
| 10:8 | TAG_UPW | **Priority Tag User Priority Weight** |
| 7 | REV4 | **Reserved** |
| 6:4 | STAG_UPW | **Special Tag User Priority Weight** |
| 3 | REV5 | **Reserved** |
| 2:0 | ACL_UPW | **ACL User Priority Weight (ACL Hit)** |

**00000048 PEM1 User Priority Egress Mapping I 08480240**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | | TAG_PRI_1 | | | QUE_CPU_1 | | | QUE_LAN_1 | | DSCP_PRI_1 | | | | | |
| Type | DC | | RW | | | RW | | | RW | | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | REV1 | | TAG_PRI_0 | | | QUE_CPU_0 | | | QUE_LAN_0 | | DSCP_PRI_0 | | | | | |
| Type | DC | | RW | | | RW | | | RW | | RW | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:30 | REV0 | **Reserved** |
| 29:27 | TAG_PRI_1 | **User Priority 1 Priority Tag Value** |
| 26:24 | QUE_CPU_1 | **User Priority 1 CPU Queue Selectio** |
| 23:22 | QUE_LAN_1 | **User Priority 1 LAN Queue Selection** |
| 21:16 | DSCP_PRI_1 | **User Priority 1 DSCP Value** |
| 15:14 | REV1 | **Reserved** |
| 13:11 | TAG_PRI_0 | **User Priority 0 Priority Tag Value** |
| 10:8 | QUE_CPU_0 | **User Priority 0 CPU Queue Selectio** |
| 7:6 | QUE_LAN_0 | **User Priority 0 LAN Queue Selection** |
| 5:0 | DSCP_PRI_0 | **User Priority 0 DSCP Value** |

**0000004C PEM2 User Priority Egress Mapping II 1B581110**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | REV0 | | TAG_PRI_3 | | | QUE_CPU_3 | | | QUE_LAN_3 | | DSCP_PRI_3 | | | | | |
| Type | DC | | RW | | | RW | | | RW | | RW | | | | | |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | REV1 | | TAG_PRI_2 | | | QUE_CPU_2 | | | QUE_LAN_2 | | DSCP_PRI_2 | | | | | |
| Type | DC | | RW | | | RW | | | RW | | RW | | | | | |
| Reset | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:30 | REV0 | **Reserved** |
| 29:27 | TAG_PRI_3 | **User Priority 3 Priority Tag Value** |
| 26:24 | QUE_CPU_3 | **User Priority 3 CPU Queue Selectio** |
| 23:22 | QUE_LAN_3 | **User Priority 3 LAN Queue Selection** |
| 21:16 | DSCP_PRI_3 | **User Priority 3 DSCP Value** |
| 15:14 | REV1 | **Reserved** |
| 13:11 | TAG_PRI_2 | **User Priority 2 Priority Tag Value** |
| 10:8 | QUE_CPU_2 | **User Priority 2 CPU Queue Selectio** |
| 7:6 | QUE_LAN_2 | **User Priority 2 LAN Queue Selection** |
| 5:0 | DSCP_PRI_2 | **User Priority 2 DSCP Value** |

**00001000 MMSCR0_Q0P0 Max-Min Scheduler Control Register 0 of Queue 0/Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q0_P0 | | | | | | | | | | | | | | | |

| Type | RW | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q0_P0 | | | | MIN_RATE_CTRL_EXP_Q0_P0 | | | | | MIN_RATE_CTRL_MAN_Q0_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q0_P0 | **Port 0 Queue 0 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q0_P0 | **Port 0 Queue 0 minimum shaper rate limit control is enabled.**<br>0: Queue 0 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass (infinite rate).<br>1: Queue 0 min. rate limit control is enabled. |
| 11:8 | MIN_RATE_CTRL_EXP_Q0_P0 | **Exponent part of Port 0 Queue 0 min. shaper rate limit control**<br>Value range: 0..4 |
| 6:0 | MIN_RATE_CTRL_MAN_Q0_P0 | **Mantissa part of Port 0 Queue 0 min. shaper rate limit control**<br>Value range: 1..100 |

## 00001004 MMSCR1_Q0P0 Max-Min Scheduler Control Register 1 of Queue 0/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q0_P0 | | | | MAX_WEIGHT_Q0_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q0_P0 | | | | MAX_RATE_CTRL_EXP_Q0_P0 | | | | | MAX_RATE_CTRL_MAN_Q0_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q0_P0 | **Port 0 Queue 0 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q0_P0 | **Port 0 Queue 0 weighted value for maximum WFQ weighted value is (q0_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q0_P0 | **Port 0 Queue 0 maximum shaper rate limit control is enabled.**<br>0: Queue 0 maximum shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate).<br>1: Queue 0 maximum shaper rate limit is enabled. |
| 11:8 | MAX_RATE_CTRL_EXP_Q0_P0 | **Exponent part of Port 0 Queue 0 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q0_P0 | **Mantissa part of Port 0 Queue 0 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001008 MMSCR0_Q1P0 Max-Min Scheduler Control Register 0 of Queue 1/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q1_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q1_P0 | | | | MIN_RATE_CTRL_EXP_Q1_P0 | | | | | MIN_RATE_CTRL_MAN_Q1_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q1_P0 | **Port 0 Queue 1 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q1_P0 | **Port 0 Queue 1 minimum shaper rate limit control is enabled.**<br>0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 1 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q1_P0 | **Exponent part of Port 0 Queue 1 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q1_P0 | **Mantissa part of Port 0 Queue 1 min. shaper rate limit control**<br>Value range: 1..127 |

## 0000100C MMSCR1_Q1P0 Max-Min Scheduler Control Register 1 of Queue 1/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q1_P0 | | | | MAX_WEIGHT_Q1_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q1_P0 | | | | MAX_RATE_CTRL_EXP_Q1_P0 | | | | | MAX_RATE_CTRL_MAN_Q1_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q1_P0 | **Port 0 Queue 1 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q1_P0 | **Port 0 Queue 1 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q1_P0 | **Port 0 Queue 1 maximum shaper rate limit control is enabled.**<br>0: Queue 1 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 1 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q1_P0 | **Exponent part of Port 0 Queue 1 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |

| | | |
|---|---|---|
| 6:0 | MAX_RATE_CTRL_MAN_Q1_P0 | **Mantissa part of Port 0 Queue 1 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001010 MMSCR0_Q2P0 Max-Min Scheduler Control Register 0 of Queue 2/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q2_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q2_P0 | | | | MIN_RATE_CTRL_EXP_Q2_P0 | | | | | MIN_RATE_CTRL_MAN_Q2_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q2_P0 | **Port 0 Queue 2 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q2_P0 | **Port 0 Queue 2 minimum shaper rate limit control is enabled.**<br>0: Queue 1 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 1 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q2_P0 | **Exponent part of Port 0 Queue 2 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q2_P0 | **Mantissa part of Port 0 Queue 2 min. shaper rate limit control**<br>Value range: 1..127 |

## 00001014 MMSCR1_Q2P0 Max-Min Scheduler Control Register 1 of Queue 2/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q2_P0 | | | | MAX_WEIGHT_Q2_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q2_P0 | | | | MAX_RATE_CTRL_EXP_Q2_P0 | | | | | MAX_RATE_CTRL_MAN_Q2_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q2_P0 | **Port 0 Queue 2 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q2_P0 | **Port 0 Queue 2 weighted value for maximum WFQ weighted value is (q1_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q2_P0 | **Port 0 Queue 2 maximum shaper rate limit control is enabled.**<br>0: Queue 2 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate) |

| | | |
|---|---|---|
| | | 1: Queue 2 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q2_P0 | **Exponent part of Port 0 Queue 2 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q2_P0 | **Mantissa part of Port 0 Queue 2 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001018 MMSCR0_Q3P0 Max-Min Scheduler Control Register 0 of Queue 3/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q3_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q3_P0 | | | | MIN_RATE_CTRL_EXP_Q3_P0 | | | | | MIN_RATE_CTRL_MAN_Q3_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q3_P0 | **Port 0 Queue 3 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q3_P0 | **Port 0 Queue 3 minimum shaper rate limit control is enabled.**<br>0: Queue 3 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 3 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q3_P0 | **Exponent part of Port 0 Queue 3 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q3_P0 | **Mantissa part of Port 0 Queue 3 min. shaper rate limit control**<br>Value range: 1..127 |

## 0000101C MMSCR1_Q3P0 Max-Min Scheduler Control Register 1 of Queue 3/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q3_P0 | | | | MAX_WEIGHT_Q3_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q3_P0 | | | | MAX_RATE_CTRL_EXP_Q3_P0 | | | | | MAX_RATE_CTRL_MAN_Q3_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q3_P0 | **Port 0 Queue 3 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |

| | | |
|---|---|---|
| 27:24 | MAX_WEIGHT_Q3_P0 | **Port 0 Queue 3 weighted value for maximum WFQ weighted value is (q3_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q3_P0 | **Port 0 Queue 3 maximum shaper rate limit control is enabled.**<br>0: Queue 3 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 3 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q3_P0 | **Exponent part of Port 0 Queue 3 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q3_P0 | **Mantissa part of Port 0 Queue 3 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001020 MMSCR0_Q4P0 Max-Min Scheduler Control Register 0 of Queue 4/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q4_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q4_P0 | | | | MIN_RATE_CTRL_EXP_Q4_P0 | | | | | MIN_RATE_CTRL_MAN_Q4_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q4_P0 | **Port 0 Queue 4 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q4_P0 | **Port 0 Queue 4 minimum shaper rate limit control is enabled.**<br>0: Queue 4 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 4 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q4_P0 | **Exponent part of Port 0 Queue 4 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q4_P0 | **Mantissa part of Port 0 Queue 4 min. shaper rate limit control**<br>Value range: 1..127 |

## 00001024 MMSCR1_Q4P0 Max-Min Scheduler Control Register 1 of Queue 4/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q4_P0 | | | | MAX_WEIGHT_Q4_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q4_P0 | | | | MAX_RATE_CTRL_EXP_Q4_P0 | | | | | MAX_RATE_CTRL_MAN_Q4_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|

| | | |
|---|---|---|
| 31 | MAX_SP_WFQ_Q4_P0 | **Port 0 Queue 4 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q4_P0 | **Port 0 Queue 4 weighted value for maximum WFQ weighted value is (q4_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q4_P0 | **Port 0 Queue 4 maximum shaper rate limit control is enabled.**<br>0: Queue 4 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 4 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q4_P0 | **Exponent part of Port 0 Queue 4 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q4_P0 | **Mantissa part of Port 0 Queue 4 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

**00001028** **MMSCR0_Q5P0** **Max-Min Scheduler Control Register 0 of Queue 5/Port 0** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q5_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q5_P0 | | | | MIN_RATE_CTRL_EXP_Q5_P0 | | | | | MIN_RATE_CTRL_MAN_Q5_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q5_P0 | **Port 0 Queue 5 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q5_P0 | **Port 0 Queue 5 minimum shaper rate limit control is enabled.**<br>0: Queue 5 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 5 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q5_P0 | **Exponent part of Port 0 Queue 5 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q5_P0 | **Mantissa part of Port 0 Queue 5 min. shaper rate limit control**<br>Value range: 1..127 |

**0000102C** **MMSCR1_Q5P0** **Max-Min Scheduler Control Register 1 of Queue 5/Port 0** **00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q5_P0 | | | | MAX_WEIGHT_Q5_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q5_P0 | | | | MAX_RATE_CTRL_EXP_Q5_P0 | | | | | MAX_RATE_CTRL_MAN_Q5_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q5_P0 | **Port 0 Queue 5 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q5_P0 | **Port 0 Queue 5 weighted value for maximum WFQ weighted value is (q5_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q5_P0 | **Port 0 Queue 5 maximum shaper rate limit control is enabled.**<br>0: Queue 5 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 5 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q5_P0 | **Exponent part of Port 0 Queue 5 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q5_P0 | **Mantissa part of Port 0 Queue 5 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

**00001030 MMSCR0_Q6P0 Max-Min Scheduler Control Register 0 of Queue 6/Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q6_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q6_P0 | | | | MIN_RATE_CTRL_EXP_Q6_P0 | | | | | MIN_RATE_CTRL_MAN_Q6_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q6_P0 | **Port 0 Queue 6 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q6_P0 | **Port 0 Queue 6 minimum shaper rate limit control is enabled.**<br>0: Queue 6 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 6 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q6_P0 | **Exponent part of Port 0 Queue 6 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q6_P0 | **Mantissa part of Port 0 Queue 6 min. shaper rate limit control**<br>Value range: 1..127 |

**00001034 MMSCR1_Q6P0 Max-Min Scheduler Control Register 1 of Queue 6/Port 0 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q6_P0 | | | | MAX_WEIGHT_Q6_P0 | | | | | | | | | | | |
| Type | RW | | | | RW | | | | | | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q | | | | MAX_RATE_CTRL_EXP_Q6_P0 | | | | | MAX_RATE_CTRL_MAN_Q6_P0 | | | | | | |

| | 6_P0 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q6_P0 | **Port 0 Queue 6 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q6_P0 | **Port 0 Queue 6 weighted value for maximum WFQ weighted value is (q6_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q6_P0 | **Port 0 Queue 6 maximum shaper rate limit control is enabled.**<br>0: Queue 6 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 6 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q6_P0 | **Exponent part of Port 0 Queue 6 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q6_P0 | **Mantissa part of Port 0 Queue 6 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001038 MMSCR0_Q7P0 Max-Min Scheduler Control Register 0 of Queue 7/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MIN_SP_WRR_Q7_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MIN_RATE_EN_Q7_P0 | | | | MIN_RATE_CTRL_EXP_Q7_P0 | | | | | MIN_RATE_CTRL_MAN_Q7_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MIN_SP_WRR_Q7_P0 | **Port 0 Queue 7 min. traffic arbitration scheme**<br>0: Strict Priority (SP)<br>1: Round-Robin (RR) |
| 15 | MIN_RATE_EN_Q7_P0 | **Port 0 Queue 7 minimum shaper rate limit control is enabled.**<br>0: Queue 7 min. rate limit control is disabled, when it is disabled, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 7 min. rate limit control enable |
| 11:8 | MIN_RATE_CTRL_EXP_Q7_P0 | **Exponent part of Port 0 Queue 7 min. shaper rate limit control**<br>Value range: 0..13 |
| 6:0 | MIN_RATE_CTRL_MAN_Q7_P0 | **Mantissa part of Port 0 Queue 7 min. shaper rate limit control**<br>Value range: 1..127 |

## 0000103C MMSCR1_Q7P0 Max-Min Scheduler Control Register 1 of Queue 7/Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MAX_SP_WFQ_Q7_P0 | | | | MAX_WEIGHT_Q7_P0 | | | | | | | | | | | |

| Type | RW | | | | RW | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | MAX_RATE_EN_Q7_P0 | | | | MAX_RATE_CTRL_EXP_Q7_P0 | | | | | MAX_RATE_CTRL_MAN_Q7_P0 | | | | | | |
| Type | RW | | | | RW | | | | | RW | | | | | | |
| Reset | 0 | | | | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31 | MAX_SP_WFQ_Q7_P0 | **Port 0 Queue 7 maximum traffic arbitration scheme**<br>0: Weighted Fair Queuing (WFQ)<br>1: Strict Priority (SP) |
| 27:24 | MAX_WEIGHT_Q7_P0 | **Port 0 Queue 7 weighted value for maximum WFQ weighted value is (q7_max_weight+1'b1)** |
| 15 | MAX_RATE_EN_Q7_P0 | **Port 0 Queue 7 maximum shaper rate limit control is enabled.**<br>0: Queue 7 maximum rate limit control disable, shaper will always let the pkt pass.(infinite rate)<br>1: Queue 7 maximum rate limit enable |
| 11:8 | MAX_RATE_CTRL_EXP_Q7_P0 | **Exponent part of Port 0 Queue 7 maximum shaper rate limit control**<br>Value range: 0..13 (4-bit) |
| 6:0 | MAX_RATE_CTRL_MAN_Q7_P0 | **Mantissa part of Port 0 Queue 7 maximum shaper rate limit control**<br>Value range: 0..127 (7-bit) |

## 00001040 ERLCR_P0 Egress Rate Limit Control Register of Port 0 00000000

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | EGC_RATE_CIR_15_0_P0 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | EG_RATE_LIMIT_EN_P0 | | | EGC_RATE_CIR_16_P0 | EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0 | | | | EGC_TB_EN_P0 | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 | | | | | | |
| Type | RW | | | RW | RW | | | | RW | RW | | | | | | |
| Reset | 0 | | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:16 | EGC_RATE_CIR_15_0_P0 | **Total 17 bits EGC_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps** |
| 15 | EG_RATE_LIMIT_EN_P0 | **EXP: egress_rate_limit_exp**<br>MAN: egress_rate_limit_man<br>Egress port rate limitation: MAN*10^(EXP)*1Kbps<br>0: Egress rate limit control disable<br>1: Enable |
| 12 | EGC_RATE_CIR_16_P0 | **Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value** |
| 11:8 | EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0 | **Exponent part of port 0 ingress rate limit control value range: 0..13 (4-bit),**<br>When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement,<br>0: 1/128ms<br>1: 1/64ms<br>2: 1/32ms<br>3: 1/16ms<br>4: 1/8ms<br>5: 1/4ms<br>6: 1/2ms<br>7: 1ms<br>8: 2ms |

| | | |
|---|---|---|
| | | 9: 4ms<br>10: 8ms<br>11: 16ms<br>12: 32ms<br>13: 64ms<br>14: 128ms<br>15: 128ms |
| 7 | EGC_TB_EN_P0 | **When this bit is disabled, the Egress rate control acts like a leaky bucket principle.**<br>Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction.<br>0: CIR/CBS mode token bucket Disable<br>1: Token bucket mode Enable |
| 6:0 | EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0 | **Mantissa part of port 0 Egress rate limit control Value range: 0..127 (7-bit),**<br>when EGC_TB_EN = 1, support maximum bucket size CBS 512 Bytes stepping, and Token Bucket = Max ( EGC_CIR*EGC_TB_T, EGC_TB_CBS*512 ) |

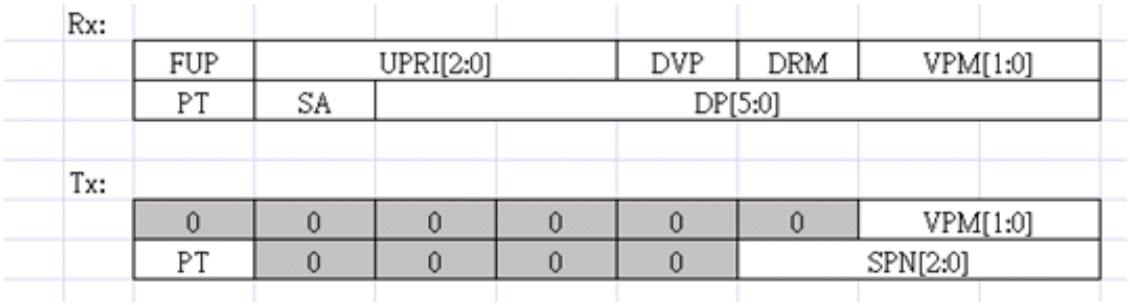
**000010E0** **GERLCR** **Global Egress Rate Limit Control Register** **00000104**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |
| Type | | | | | | | | | | | | | | | | |
| Reset | | | | | | | | | | | | | | | | |
| **Bit** | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| **Name** | | | | | | | **EGC_MFRM_EX** | **EGC_IPG_OP** | **EGC_IPG_BYTE** | | | | | | | |
| **Type** | | | | | | | RW | RW | RW | | | | | | | |
| **Reset** | | | | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 9 | EGC_MFRM_EX | **When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers)**<br>0: Include management frames<br>1: Exclude management frames |
| 8 | EGC_IPG_OP | **Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation.**<br>0: IPG byte is excluded<br>1: IPG byte is included |
| 7:0 | EGC_IPG_BYTE | **Egress Rate IPG Byte Count**<br>Byte count should be added while calculating the rate limit.<br>0x04: 4 byte CRC (default)<br>0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble |

## 2.19 Special tag format

Special is used for taking the per-port information to CPU port. It replaces the VLAN tag and inserts the special tag format as below:




**RX**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | FUP | UPR[2:0] | | | DVP | DRM | VPM[1:0] | |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | PT | SA | DP[5:0] | | | | | |

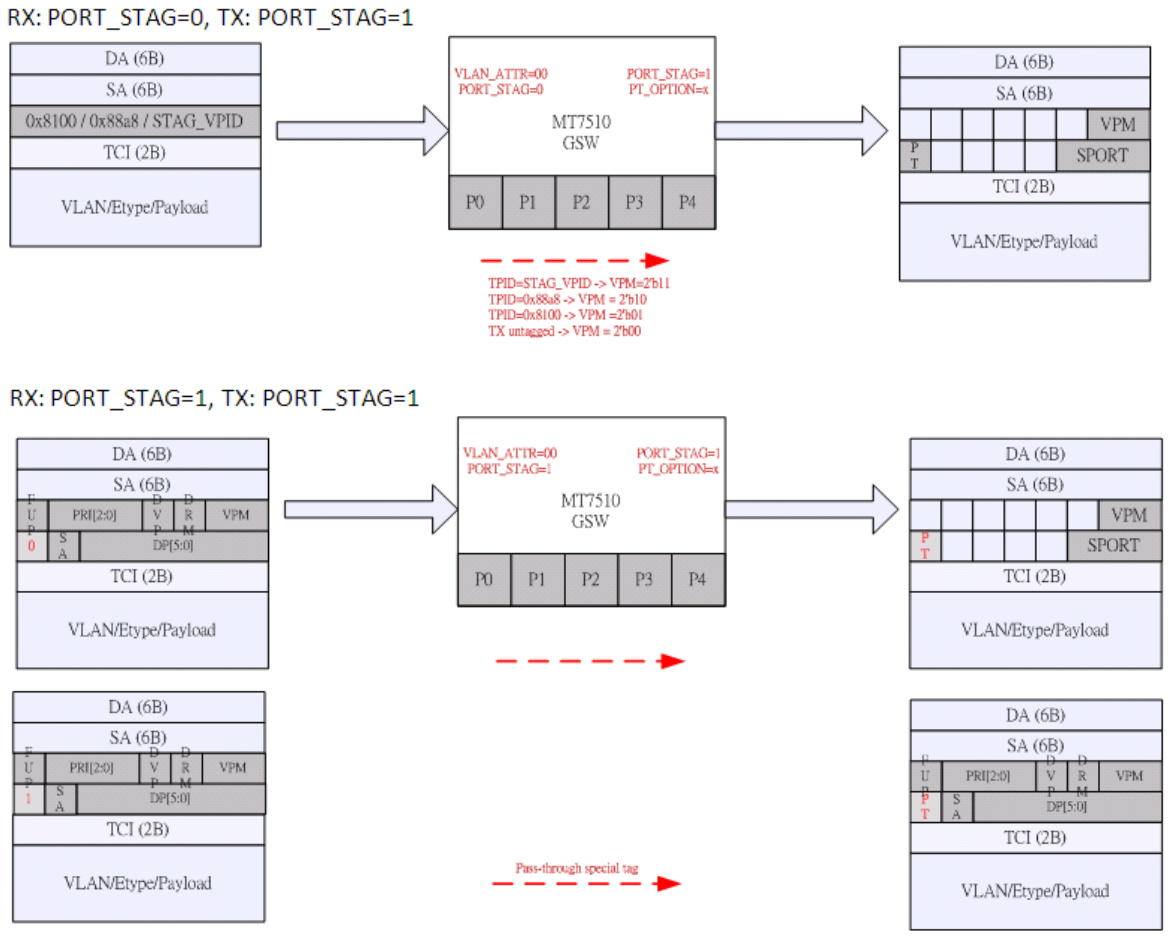
| Bit(s) | Name | Description |
|---|---|---|
| 15 | FUP | **Force PPE user priority** |
| 14:12 | UPR | PPE user priority |
| 11 | DVP | Disable VALN priority remarking |
| 10 | DRM | Disable DSCP priority remarking |
| 9:8 | VPM | Tag attribute before special tag insertion;<br>2'b00 untagged;<br>2'b01 TPID=8100;<br>2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8) |
| 7 | PT | Pass through |
| 6 | SA | Disable SA learning |
| 5:0 | DP | Force forwarding port map; all 0 means disable. |

**TX**

| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| Name | 0 | 0 | 0 | 0 | 0 | 0 | VPM[1:0] | |
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| Name | PT | 0 | 0 | 0 | 0 | SPN[2:0] | | |

| Bit(s) | Name | Description |
|---|---|---|
| 9:8 | VPM | Tag attribute before special tag insertion;<br>2'b00 untagged;<br>2'b01 TPID=8100;<br>2'b10 TPID=predefined (e.g. 0x9100 or 0x88a8) |
| 7 | PT | Pass through<br>Disable VALN priority remarking |
| 2:0 | SPN | Source port number |

We show some case here to explain the behavior of special tag:




You can enable them at Reg 0x2010,0x2110…etc.., for per-port ability.

**00002010 PVC Port VLAN Control of P0 000000C0**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | STAG_VPID | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DIS_PVID | FORCE_PVID | REV0 | PT_VPM | PT_OPTION | EG_TAG | | | VLAN_ATTR | | PORT_STAG | BC_LKYV_EN | MC_LKYV_EN | UC_LKYV_EN | ACC_FRM | |
| Type | RW | RW | DC | RW | RW | RW | | | RW | | RW | RW | RW | RW | RW | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

## 2.20 Local port enable

This is used for debugging not for normal use. It means it would add the self port to the MAC table. So, the same packet would come out from the input port. Set 7th of 0x000c to enable it.

**0000000C AGC ARL Global Control 00071819**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | MLDv2_int_en | REV0 | | | | | | | | | | | | ACL_INT | VLAN_INT | ADDR_INT |
| Type | RW | DC | | | | | | | | | | | | RO | RO | RO |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | RATE_COMP | COMP_BNUM | | | | | | | LOCAL_EN | ARL_PADDING | ACL_MULTI | L2LEN_CHK | CTRL_DROP | VLAN4CPU | ARL_PRI | ALR_RST_N |
| Type | RW | RW | | | | | | | RW | RW | RW | RW | RW | RW | RW | RW |
| Reset | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |

## 2.21 System MAC Controller

GSW build-in the internal MAC. The default MAC is 00000017a501. We put them at 0x30E8 and 0x30E4. You can change the default value as you want.

**000030E4 SMACCR0 System MAC Control Register 0 0017A501**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | SMACCR0[31:16] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SMACCR0[15:0] | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| Bit(s) | Name | Description |
|---|---|---|
| 31:0 | SMACCR0 | **System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame.** |

**000030E8 SMACCR1 System MAC Control Register 1 00000000**

| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | | | | | | | | | |
| Type | | | | | | | | | | | | | | | | |
| Reset | | | | | | | | | | | | | | | | |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SMACCR1 | | | | | | | | | | | | | | | |
| Type | RW | | | | | | | | | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bit(s) | Name | Description |
|---|---|---|
| 15:0 | SMACCR1 | **System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame.** |

## 2.22 MIB (management information base) counter

MIB counters are used to record the packet number of ingress and egress port. You can use software reset to clean it. Or write 0x4fe0 as 0 then write 80000000 to restart it.

### MIB counter of port 0:

| | | | |
|---|---|---|---|
| 00004000 | TDPC_P0 | 32 | TX Drop Packet Counter of Port 0 |
| 00004004 | TCRC_P0 | 32 | TX CRC Packet Counter of Port 0 |
| 00004008 | TUPC_P0 | 32 | TX Unicast Packet Counter of Port 0 |
| 0000400C | TMPC_P0 | 32 | TX Multicast Packet Counter of Port 0 |
| 00004010 | TBPC_P0 | 32 | TX Broadcast Packet Counter of Port 0 |
| 00004014 | TCEC_P0 | 32 | TX Collision Event Counter of Port 0 |
| 00004018 | TSCEC_P0 | 32 | TX Single Collision Event Counter of Port 0 |
| 0000401C | TMCEC_P0 | 32 | TX Multiple Collision Event Counter of Port 0 |
| 00004020 | TDEC_P0 | 32 | TX Deferred Event Counter of Port 0 |
| 00004024 | TLCEC_P0 | 32 | TX Late Collision Event Counter of Port 0 |
| 00004028 | TXCEC_P0 | 32 | TX excessive Collision Event Counter of Port 0 |
| 0000402C | TPPC_P0 | 32 | TX Pause Packet Counter of Port 0 |
| 00004030 | TL64PC_P0 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 0 |
| 00004034 | TL65PC_P0 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 0 |
| 00004038 | TL128PC_P0 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 0 |
| 0000403C | TL256PC_P0 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 0 |
| 00004040 | TL512PC_P0 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 0 |
| 00004044 | TL1024PC_P0 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 0 |
| 00004048 | TOCL_P0 | 32 | TX Octet Counter Low double word of Port 0 |
| 0000404C | TOCH_P0 | 32 | TX Octet Counter High double word of Port 0 |
| 00004060 | RDPC_P0 | 32 | RX Drop Packet Counter of Port 0 |
| 00004064 | RFPC_P0 | 32 | RX Filtering Packet Counter of Port 0 |
| 00004068 | RUPC_P0 | 32 | RX Unicast Packet Counter of Port 0 |
| 0000406C | RMPC_P0 | 32 | RX Multicast Packet Counter of Port 0 |
| 00004070 | RBPC_P0 | 32 | RX Broadcast Packet Counter of Port 0 |
| 00004074 | RAEPC_P0 | 32 | RX Alignment Error Packet Counter of Port 0 |
| 00004078 | RCEPC_P0 | 32 | RX CRC(FCS) Error Packet Counter of Port 0 |
| 0000407C | RUSPC_P0 | 32 | RX Undersize Packet Counter of Port 0 |
| 00004080 | RFEPC_P0 | 32 | RX Fragment Error Packet Counter of Port 0 |
| 00004084 | ROSPC_P0 | 32 | RX Oversize Packet Counter of Port 0 |
| 00004088 | RJEPC_P0 | 32 | RX Jabber Error Packet Counter of Port 0 |
| 0000408C | RPPC_P0 | 32 | RX Pause Packet Counter of Port 0 |
| 00004090 | RL64PC_P0 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 0 |
| 00004094 | RL65PC_P0 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 0 |
| 00004098 | RL128PC_P0 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 0 |
| 0000409C | RL256PC_P0 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 0 |
| 000040A0 | RL512PC_P0 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 0 |
| 000040A4 | RL1024PC_P0 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 0 |
| 000040A8 | ROCL_P0 | 32 | RX Octet Counter Low double word of Port 0 |

| | | | |
|---|---|---|---|
| 000040AC | ROCH_P0 | 32 | Rx Octet Counter High double word of Port 0 |
| 000040B0 | RDPC_CTRL_P0 | 32 | RX CTRL Drop Packet Counter of Port 0 |
| 000040B4 | RDPC_ING_P0 | 32 | RX Ingress Drop Packet Counter of Port 0 |
| 000040B8 | RDPC_ARL_P0 | 32 | RX ARL Drop Packet Counter of Port 0 |
| 000040D0 | TMIB_HF_STS_P0 | 32 | TX Port MIB Counter Half Full Status of Port 0 |
| 000040D4 | RMIB_HF_STS_P0 | 32 | RX Port MIB Counter Half Full Status of Port 0 |

## MIB counter of port 1:

| | | | |
|---|---|---|---|
| 00004100 | TDPC_P1 | 32 | TX Drop Packet Counter of Port 1 |
| 00004104 | TCRC_P1 | 32 | TX CRC Packet Counter of Port 1 |
| 00004108 | TUPC_P1 | 32 | TX Unicast Packet Counter of Port 1 |
| 0000410C | TMPC_P1 | 32 | TX Multicast Packet Counter of Port 1 |
| 00004110 | TBPC_P1 | 32 | TX Broadcast Packet Counter of Port 1 |
| 00004114 | TCEC_P1 | 32 | TX Collision Event Counter of Port 1 |
| 00004118 | TSCEC_P1 | 32 | TX Single Collision Event Counter of Port 1 |
| 0000411C | TMCEC_P1 | 32 | TX Multiple Collision Event Counter of Port 1 |
| 00004120 | TDEC_P1 | 32 | TX Deferred Event Counter of Port 1 |
| 00004124 | TLCEC_P1 | 32 | TX Late Collision Event Counter of Port 1 |
| 00004128 | TXCEC_P1 | 32 | TX excessive Collision Event Counter of Port 1 |
| 0000412C | TPPC_P1 | 32 | TX Pause Packet Counter of Port 1 |
| 00004130 | TL64PC_P1 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 1 |
| 00004134 | TL65PC_P1 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 1 |
| 00004138 | TL128PC_P1 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 1 |
| 0000413C | TL256PC_P1 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 1 |
| 00004140 | TL512PC_P1 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 1 |
| 00004144 | TL1024PC_P1 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 1 |
| 00004148 | TOCL_P1 | 32 | TX Octet Counter Low double word of Port 1 |
| 0000414C | TOCH_P1 | 32 | TX Octet Counter High double word of Port 1 |
| 00004160 | RDPC_P1 | 32 | RX Drop Packet Counter of Port 1 |
| 00004164 | RFPC_P1 | 32 | RX Filtering Packet Counter of Port 1 |
| 00004168 | RUPC_P1 | 32 | RX Unicast Packet Counter of Port 1 |
| 0000416C | RMPC_P1 | 32 | RX Multicast Packet Counter of Port 1 |
| 00004170 | RBPC_P1 | 32 | RX Broadcast Packet Counter of Port 1 |
| 00004174 | RAEPC_P1 | 32 | RX Alignment Error Packet Counter of Port 1 |
| 00004178 | RCEPC_P1 | 32 | RX CRC(FCS) Error Packet Counter of Port 1 |
| 0000417C | RUSPC_P1 | 32 | RX Undersize Packet Counter of Port 1 |
| 00004180 | RFEPC_P1 | 32 | RX Fragment Error Packet Counter of Port 1 |
| 00004184 | ROSPC_P1 | 32 | RX Oversize Packet Counter of Port 1 |
| 00004188 | RJEPC_P1 | 32 | RX Jabber Error Packet Counter of Port 1 |
| 0000418C | RPPC_P1 | 32 | RX Pause Packet Counter of Port 1 |
| 00004190 | RL64PC_P1 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 1 |
| 00004194 | RL65PC_P1 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 1 |
| 00004198 | RL128PC_P1 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 1 |
| 0000419C | RL256PC_P1 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 1 |

| | | | |
|---|---|---|---|
| 000041A0 | RL512PC_P1 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 1 |
| 000041A4 | RL1024PC_P1 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 1 |
| 000041A8 | ROCL_P1 | 32 | RX Octet Counter Low double word of Port 1 |
| 000041AC | ROCH_P1 | 32 | Rx Octet Counter High double word of Port 1 |
| 000041B0 | RDPC_CTRL_P1 | 32 | RX CTRL Drop Packet Counter of Port 1 |
| 000041B4 | RDPC_ING_P1 | 32 | RX Ingress Drop Packet Counter of Port 1 |
| 000041B8 | RDPC_ARL_P1 | 32 | RX ARL Drop Packet Counter of Port 1 |
| 000041D0 | TMIB_HF_STS_P1 | 32 | TX Port MIB Counter Half Full Status of Port 1 |
| 000041D4 | RMIB_HF_STS_P1 | 32 | RX Port MIB Counter Half Full Status of Port 1 |

## MIB counter of port 2:

| | | | |
|---|---|---|---|
| 00004200 | TDPC_P2 | 32 | TX Drop Packet Counter of Port 2 |
| 00004204 | TCRC_P2 | 32 | TX CRC Packet Counter of Port 2 |
| 00004208 | TUPC_P2 | 32 | TX Unicast Packet Counter of Port 2 |
| 0000420C | TMPC_P2 | 32 | TX Multicast Packet Counter of Port 2 |
| 00004210 | TBPC_P2 | 32 | TX Broadcast Packet Counter of Port 2 |
| 00004214 | TCEC_P2 | 32 | TX Collision Event Counter of Port 2 |
| 00004218 | TSCEC_P2 | 32 | TX Single Collision Event Counter of Port 2 |
| 0000421C | TMCEC_P2 | 32 | TX Multiple Collision Event Counter of Port 2 |
| 00004220 | TDEC_P2 | 32 | TX Deferred Event Counter of Port 2 |
| 00004224 | TLCEC_P2 | 32 | TX Late Collision Event Counter of Port 2 |
| 00004228 | TXCEC_P2 | 32 | TX excessive Collision Event Counter of Port 2 |
| 0000422C | TPPC_P2 | 32 | TX Pause Packet Counter of Port 2 |
| 00004230 | TL64PC_P2 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 2 |
| 00004234 | TL65PC_P2 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 2 |
| 00004238 | TL128PC_P2 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 2 |
| 0000423C | TL256PC_P2 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 2 |
| 00004240 | TL512PC_P2 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 2 |
| 00004244 | TL1024PC_P2 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 2 |
| 00004248 | TOCL_P2 | 32 | TX Octet Counter Low double word of Port 2 |
| 0000424C | TOCH_P2 | 32 | TX Octet Counter High double word of Port 2 |
| 00004260 | RDPC_P2 | 32 | RX Drop Packet Counter of Port 2 |
| 00004264 | RFPC_P2 | 32 | RX Filtering Packet Counter of Port 2 |
| 00004268 | RUPC_P2 | 32 | RX Unicast Packet Counter of Port 2 |
| 0000426C | RMPC_P2 | 32 | RX Multicast Packet Counter of Port 2 |
| 00004270 | RBPC_P2 | 32 | RX Broadcast Packet Counter of Port 2 |
| 00004274 | RAEPC_P2 | 32 | RX Alignment Error Packet Counter of Port 2 |
| 00004278 | RCEPC_P2 | 32 | RX CRC(FCS) Error Packet Counter of Port 2 |
| 0000427C | RUSPC_P2 | 32 | RX Undersize Packet Counter of Port 2 |
| 00004280 | RFEPC_P2 | 32 | RX Fragment Error Packet Counter of Port 2 |
| 00004284 | ROSPC_P2 | 32 | RX Oversize Packet Counter of Port 2 |
| 00004288 | RJEPC_P2 | 32 | RX Jabber Error Packet Counter of Port 2 |
| 0000428C | RPPC_P2 | 32 | RX Pause Packet Counter of Port 2 |
| 00004290 | RL64PC_P2 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 2 |

| | | | |
|---|---|---|---|
| 00004294 | RL65PC_P2 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 2 |
| 00004298 | RL128PC_P2 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 2 |
| 0000429C | RL256PC_P2 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 2 |
| 000042A0 | RL512PC_P2 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 2 |
| 000042A4 | RL1024PC_P2 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 2 |
| 000042A8 | ROCL_P2 | 32 | RX Octet Counter Low double word of Port 2 |
| 000042AC | ROCH_P2 | 32 | Rx Octet Counter High double word of Port 2 |
| 000042B0 | RDPC_CTRL_P2 | 32 | RX CTRL Drop Packet Counter of Port 2 |
| 000042B4 | RDPC_ING_P2 | 32 | RX Ingress Drop Packet Counter of Port 2 |
| 000042B8 | RDPC_ARL_P2 | 32 | RX ARL Drop Packet Counter of Port 2 |
| 000042D0 | TMIB_HF_STS_P2 | 32 | TX Port MIB Counter Half Full Status of Port 2 |
| 000042D4 | RMIB_HF_STS_P2 | 32 | RX Port MIB Counter Half Full Status of Port 2 |

## MIB counter of port 3:

| | | | |
|---|---|---|---|
| 00004300 | TDPC_P3 | 32 | TX Drop Packet Counter of Port 3 |
| 00004304 | TCRC_P3 | 32 | TX CRC Packet Counter of Port 3 |
| 00004308 | TUPC_P3 | 32 | TX Unicast Packet Counter of Port 3 |
| 0000430C | TMPC_P3 | 32 | TX Multicast Packet Counter of Port 3 |
| 00004310 | TBPC_P3 | 32 | TX Broadcast Packet Counter of Port 3 |
| 00004314 | TCEC_P3 | 32 | TX Collision Event Counter of Port 3 |
| 00004318 | TSCEC_P3 | 32 | TX Single Collision Event Counter of Port 3 |
| 0000431C | TMCEC_P3 | 32 | TX Multiple Collision Event Counter of Port 3 |
| 00004320 | TDEC_P3 | 32 | TX Deferred Event Counter of Port 3 |
| 00004324 | TLCEC_P3 | 32 | TX Late Collision Event Counter of Port 3 |
| 00004328 | TXCEC_P3 | 32 | TX excessive Collision Event Counter of Port 3 |
| 0000432C | TPPC_P3 | 32 | TX Pause Packet Counter of Port 3 |
| 00004330 | TL64PC_P3 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 3 |
| 00004334 | TL65PC_P3 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 3 |
| 00004338 | TL128PC_P3 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 3 |
| 0000433C | TL256PC_P3 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 3 |
| 00004340 | TL512PC_P3 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 3 |
| 00004344 | TL1024PC_P3 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 3 |
| 00004348 | TOCL_P3 | 32 | TX Octet Counter Low double word of Port 3 |
| 0000434C | TOCH_P3 | 32 | TX Octet Counter High double word of Port 3 |
| 00004360 | RDPC_P3 | 32 | RX Drop Packet Counter of Port 3 |
| 00004364 | RFPC_P3 | 32 | RX Filtering Packet Counter of Port 3 |
| 00004368 | RUPC_P3 | 32 | RX Unicast Packet Counter of Port 3 |
| 0000436C | RMPC_P3 | 32 | RX Multicast Packet Counter of Port 3 |
| 00004370 | RBPC_P3 | 32 | RX Broadcast Packet Counter of Port 3 |
| 00004374 | RAEPC_P3 | 32 | RX Alignment Error Packet Counter of Port 3 |
| 00004378 | RCEPC_P3 | 32 | RX CRC(FCS) Error Packet Counter of Port 3 |
| 0000437C | RUSPC_P3 | 32 | RX Undersize Packet Counter of Port 3 |
| 00004380 | RFEPC_P3 | 32 | RX Fragment Error Packet Counter of Port 3 |
| 00004384 | ROSPC_P3 | 32 | RX Oversize Packet Counter of Port 3 |

| | | | |
|---|---|---|---|
| 00004388 | RJEPC_P3 | 32 | RX Jabber Error Packet Counter of Port 3 |
| 0000438C | RPPC_P3 | 32 | RX Pause Packet Counter of Port 3 |
| 00004390 | RL64PC_P3 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 3 |
| 00004394 | RL65PC_P3 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 3 |
| 00004398 | RL128PC_P3 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 3 |
| 0000439C | RL256PC_P3 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 3 |
| 000043A0 | RL512PC_P3 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 3 |
| 000043A4 | RL1024PC_P3 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 3 |
| 000043A8 | ROCL_P3 | 32 | RX Octet Counter Low double word of Port 3 |
| 000043AC | ROCH_P3 | 32 | Rx Octet Counter High double word of Port 3 |
| 000043B0 | RDPC_CTRL_P3 | 32 | RX CTRL Drop Packet Counter of Port 3 |
| 000043B4 | RDPC_ING_P3 | 32 | RX Ingress Drop Packet Counter of Port 3 |
| 000043B8 | RDPC_ARL_P3 | 32 | RX ARL Drop Packet Counter of Port 3 |
| 000043D0 | TMIB_HF_STS_P3 | 32 | TX Port MIB Counter Half Full Status of Port 3 |
| 000043D4 | RMIB_HF_STS_P3 | 32 | RX Port MIB Counter Half Full Status of Port 3 |

## MIB counter of port 4:

| | | | |
|---|---|---|---|
| 00004400 | TDPC_P4 | 32 | TX Drop Packet Counter of Port 4 |
| 00004404 | TCRC_P4 | 32 | TX CRC Packet Counter of Port 4 |
| 00004408 | TUPC_P4 | 32 | TX Unicast Packet Counter of Port 4 |
| 0000440C | TMPC_P4 | 32 | TX Multicast Packet Counter of Port 4 |
| 00004410 | TBPC_P4 | 32 | TX Broadcast Packet Counter of Port 4 |
| 00004414 | TCEC_P4 | 32 | TX Collision Event Counter of Port 4 |
| 00004418 | TSCEC_P4 | 32 | TX Single Collision Event Counter of Port 4 |
| 0000441C | TMCEC_P4 | 32 | TX Multiple Collision Event Counter of Port 4 |
| 00004420 | TDEC_P4 | 32 | TX Deferred Event Counter of Port 4 |
| 00004424 | TLCEC_P4 | 32 | TX Late Collision Event Counter of Port 4 |
| 00004428 | TXCEC_P4 | 32 | TX excessive Collision Event Counter of Port 4 |
| 0000442C | TPPC_P4 | 32 | TX Pause Packet Counter of Port 4 |
| 00004430 | TL64PC_P4 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 4 |
| 00004434 | TL65PC_P4 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 4 |
| 00004438 | TL128PC_P4 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 4 |
| 0000443C | TL256PC_P4 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 4 |
| 00004440 | TL512PC_P4 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 4 |
| 00004444 | TL1024PC_P4 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 4 |
| 00004448 | TOCL_P4 | 32 | TX Octet Counter Low double word of Port 4 |
| 0000444C | TOCH_P4 | 32 | TX Octet Counter High double word of Port 4 |
| 00004460 | RDPC_P4 | 32 | RX Drop Packet Counter of Port 4 |
| 00004464 | RFPC_P4 | 32 | RX Filtering Packet Counter of Port 4 |
| 00004468 | RUPC_P4 | 32 | RX Unicast Packet Counter of Port 4 |
| 0000446C | RMPC_P4 | 32 | RX Multicast Packet Counter of Port 4 |
| 00004470 | RBPC_P4 | 32 | RX Broadcast Packet Counter of Port 4 |
| 00004474 | RAEPC_P4 | 32 | RX Alignment Error Packet Counter of Port 4 |
| 00004478 | RCEPC_P4 | 32 | RX CRC(FCS) Error Packet Counter of Port 4 |

| | | | |
|---|---|---|---|
| 0000447C | RUSPC_P4 | 32 | RX Undersize Packet Counter of Port 4 |
| 00004480 | RFEPC_P4 | 32 | RX Fragment Error Packet Counter of Port 4 |
| 00004484 | ROSPC_P4 | 32 | RX Oversize Packet Counter of Port 4 |
| 00004488 | RJEPC_P4 | 32 | RX Jabber Error Packet Counter of Port 4 |
| 0000448C | RPPC_P4 | 32 | RX Pause Packet Counter of Port 4 |
| 00004490 | RL64PC_P4 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 4 |
| 00004494 | RL65PC_P4 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 4 |
| 00004498 | RL128PC_P4 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 4 |
| 0000449C | RL256PC_P4 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 4 |
| 000044A0 | RL512PC_P4 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 4 |
| 000044A4 | RL1024PC_P4 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 4 |
| 000044A8 | ROCL_P4 | 32 | RX Octet Counter Low double word of Port 4 |
| 000044AC | ROCH_P4 | 32 | Rx Octet Counter High double word of Port 4 |
| 000044B0 | RDPC_CTRL_P4 | 32 | RX CTRL Drop Packet Counter of Port 4 |
| 000044B4 | RDPC_ING_P4 | 32 | RX Ingress Drop Packet Counter of Port 4 |
| 000044B8 | RDPC_ARL_P4 | 32 | RX ARL Drop Packet Counter of Port 4 |
| 000044D0 | TMIB_HF_STS_P4 | 32 | TX Port MIB Counter Half Full Status of Port 4 |
| 000044D4 | RMIB_HF_STS_P4 | 32 | RX Port MIB Counter Half Full Status of Port 4 |

# MIB counter of port 5:

| | | | |
|---|---|---|---|
| 00004500 | TDPC_P5 | 32 | TX Drop Packet Counter of Port 5 |
| 00004504 | TCRC_P5 | 32 | TX CRC Packet Counter of Port 5 |
| 00004508 | TUPC_P5 | 32 | TX Unicast Packet Counter of Port 5 |
| 0000450C | TMPC_P5 | 32 | TX Multicast Packet Counter of Port 5 |
| 00004510 | TBPC_P5 | 32 | TX Broadcast Packet Counter of Port 5 |
| 00004514 | TCEC_P5 | 32 | TX Collision Event Counter of Port 5 |
| 00004518 | TSCEC_P5 | 32 | TX Single Collision Event Counter of Port 5 |
| 0000451C | TMCEC_P5 | 32 | TX Multiple Collision Event Counter of Port 5 |
| 00004520 | TDEC_P5 | 32 | TX Deferred Event Counter of Port 5 |
| 00004524 | TLCEC_P5 | 32 | TX Late Collision Event Counter of Port 5 |
| 00004528 | TXCEC_P5 | 32 | TX excessive Collision Event Counter of Port 5 |
| 0000452C | TPPC_P5 | 32 | TX Pause Packet Counter of Port 5 |
| 00004530 | TL64PC_P5 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 5 |
| 00004534 | TL65PC_P5 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 5 |
| 00004538 | TL128PC_P5 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 5 |
| 0000453C | TL256PC_P5 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 5 |
| 00004540 | TL512PC_P5 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 5 |
| 00004544 | TL1024PC_P5 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 5 |
| 00004548 | TOCL_P5 | 32 | TX Octet Counter Low double word of Port 5 |
| 0000454C | TOCH_P5 | 32 | TX Octet Counter High double word of Port 5 |
| 00004560 | RDPC_P5 | 32 | RX Drop Packet Counter of Port 5 |
| 00004564 | RFPC_P5 | 32 | RX Filtering Packet Counter of Port 5 |
| 00004568 | RUPC_P5 | 32 | RX Unicast Packet Counter of Port 5 |
| 0000456C | RMPC_P5 | 32 | RX Multicast Packet Counter of Port 5 |

| | | | |
|---|---|---|---|
| 00004570 | RBPC_P5 | 32 | RX Broadcast Packet Counter of Port 5 |
| 00004574 | RAEPC_P5 | 32 | RX Alignment Error Packet Counter of Port 5 |
| 00004578 | RCEPC_P5 | 32 | RX CRC(FCS) Error Packet Counter of Port 5 |
| 0000457C | RUSPC_P5 | 32 | RX Undersize Packet Counter of Port 5 |
| 00004580 | RFEPC_P5 | 32 | RX Fragment Error Packet Counter of Port 5 |
| 00004584 | ROSPC_P5 | 32 | RX Oversize Packet Counter of Port 5 |
| 00004588 | RJEPC_P5 | 32 | RX Jabber Error Packet Counter of Port 5 |
| 0000458C | RPPC_P5 | 32 | RX Pause Packet Counter of Port 5 |
| 00004590 | RL64PC_P5 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 5 |
| 00004594 | RL65PC_P5 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 5 |
| 00004598 | RL128PC_P5 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 5 |
| 0000459C | RL256PC_P5 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 5 |
| 000045A0 | RL512PC_P5 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 5 |
| 000045A4 | RL1024PC_P5 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 5 |
| 000045A8 | ROCL_P5 | 32 | RX Octet Counter Low double word of Port 5 |
| 000045AC | ROCH_P5 | 32 | Rx Octet Counter High double word of Port 5 |
| 000045B0 | RDPC_CTRL_P5 | 32 | RX CTRL Drop Packet Counter of Port 5 |
| 000045B4 | RDPC_ING_P5 | 32 | RX Ingress Drop Packet Counter of Port 5 |
| 000045B8 | RDPC_ARL_P5 | 32 | RX ARL Drop Packet Counter of Port 5 |
| 000045D0 | TMIB_HF_STS_P5 | 32 | TX Port MIB Counter Half Full Status of Port 5 |
| 000045D4 | RMIB_HF_STS_P5 | 32 | RX Port MIB Counter Half Full Status of Port 5 |

## MIB counter of port 6:

| | | | |
|---|---|---|---|
| 00004600 | TDPC_P6 | 32 | TX Drop Packet Counter of Port 6 |
| 00004604 | TCRC_P6 | 32 | TX CRC Packet Counter of Port 6 |
| 00004608 | TUPC_P6 | 32 | TX Unicast Packet Counter of Port 6 |
| 0000460C | TMPC_P6 | 32 | TX Multicast Packet Counter of Port 6 |
| 00004610 | TBPC_P6 | 32 | TX Broadcast Packet Counter of Port 6 |
| 00004614 | TCEC_P6 | 32 | TX Collision Event Counter of Port 6 |
| 00004618 | TSCEC_P6 | 32 | TX Single Collision Event Counter of Port 6 |
| 0000461C | TMCEC_P6 | 32 | TX Multiple Collision Event Counter of Port 6 |
| 00004620 | TDEC_P6 | 32 | TX Deferred Event Counter of Port 6 |
| 00004624 | TLCEC_P6 | 32 | TX Late Collision Event Counter of Port 6 |
| 00004628 | TXCEC_P6 | 32 | TX excessive Collision Event Counter of Port 6 |
| 0000462C | TPPC_P6 | 32 | TX Pause Packet Counter of Port 6 |
| 00004630 | TL64PC_P6 | 32 | TX packet Length in 64-byte slot Packet Counter of Port 6 |
| 00004634 | TL65PC_P6 | 32 | TX packet Length in 65-byte slot Packet Counter of Port 6 |
| 00004638 | TL128PC_P6 | 32 | TX packet Length in 128-byte slot Packet Counter of Port 6 |
| 0000463C | TL256PC_P6 | 32 | TX packet Length in 256-byte slot Packet Counter of Port 6 |
| 00004640 | TL512PC_P6 | 32 | TX packet Length in 512-byte slot Packet Counter of Port 6 |
| 00004644 | TL1024PC_P6 | 32 | TX packet Length in 1024-byte slot Packet Counter of Port 6 |
| 00004648 | TOCL_P6 | 32 | TX Octet Counter Low double word of Port 6 |
| 0000464C | TOCH_P6 | 32 | TX Octet Counter High double word of Port 6 |

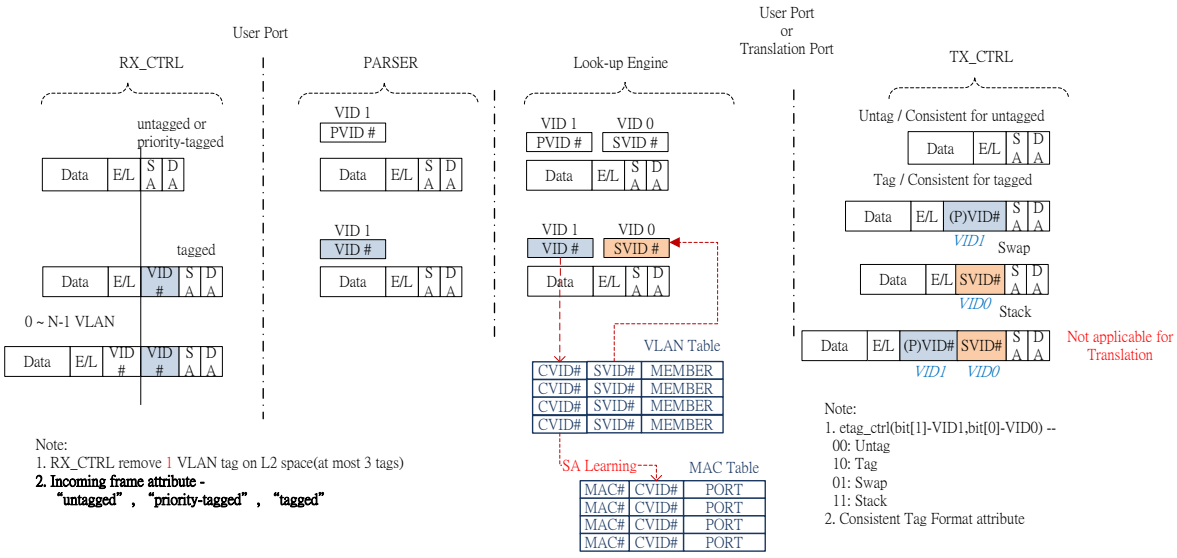
| | | | |
|---|---|---|---|
| 00004660 | RDPC_P6 | 32 | RX Drop Packet Counter of Port 6 |
| 00004664 | RFPC_P6 | 32 | RX Filtering Packet Counter of Port 6 |
| 00004668 | RUPC_P6 | 32 | RX Unicast Packet Counter of Port 6 |
| 0000466C | RMPC_P6 | 32 | RX Multicast Packet Counter of Port 6 |
| 00004670 | RBPC_P6 | 32 | RX Broadcast Packet Counter of Port 6 |
| 00004674 | RAEPC_P6 | 32 | RX Alignment Error Packet Counter of Port 6 |
| 00004678 | RCEPC_P6 | 32 | RX CRC(FCS) Error Packet Counter of Port 6 |
| 0000467C | RUSPC_P6 | 32 | RX Undersize Packet Counter of Port 6 |
| 00004680 | RFEPC_P6 | 32 | RX Fragment Error Packet Counter of Port 6 |
| 00004684 | ROSPC_P6 | 32 | RX Oversize Packet Counter of Port 6 |
| 00004688 | RJEPC_P6 | 32 | RX Jabber Error Packet Counter of Port 6 |
| 0000468C | RPPC_P6 | 32 | RX Pause Packet Counter of Port 6 |
| 00004690 | RL64PC_P6 | 32 | RX packet Length in 64-byte slot Packet Counter of Port 6 |
| 00004694 | RL65PC_P6 | 32 | RX packet Length in 65-byte slot Packet Counter of Port 6 |
| 00004698 | RL128PC_P6 | 32 | RX packet Length in 128-byte slot Packet Counter of Port 6 |
| 0000469C | RL256PC_P6 | 32 | RX packet Length in 256-byte slot Packet Counter of Port 6 |
| 000046A0 | RL512PC_P6 | 32 | RX packet Length in 512-byte slot Packet Counter of Port 6 |
| 000046A4 | RL1024PC_P6 | 32 | RX packet Length in 1024-byte slot Packet Counter of Port 6 |
| 000046A8 | ROCL_P6 | 32 | RX Octet Counter Low double word of Port 6 |
| 000046AC | ROCH_P6 | 32 | Rx Octet Counter High double word of Port 6 |
| 000046B0 | RDPC_CTRL_P6 | 32 | RX CTRL Drop Packet Counter of Port 6 |
| 000046B4 | RDPC_ING_P6 | 32 | RX Ingress Drop Packet Counter of Port 6 |
| 000046B8 | RDPC_ARL_P6 | 32 | RX ARL Drop Packet Counter of Port 6 |
| 000046D0 | TMIB_HF_STS_P6 | 32 | TX Port MIB Counter Half Full Status of Port 6 |
| 000046D4 | RMIB_HF_STS_P6 | 32 | RX Port MIB Counter Half Full Status of Port 6 |

# 3 Annex

## User Port

The user port is the default VLAN port. The incoming VLAN-tagged frame is stripped by the outer tag despite the following inner tags. Per untagged or priority-tagged frame, PVID is treated as VID1 tag. At the same time, VID1 is used to look for VLAN table to get the FID and Service tag for VID0. When a new Source MAC address is learned, the VID1 will also be learned on the MAC table.

On the TX_CTRL side, each frame carries 2*N-port egress control bits on per-port based. Bit0 indicates whether this frame carries VID 0 or not; similarly, Bit.1 is for VID1. Once "Consistent tag" is set, the egress tag format will follow the ingress tag format.

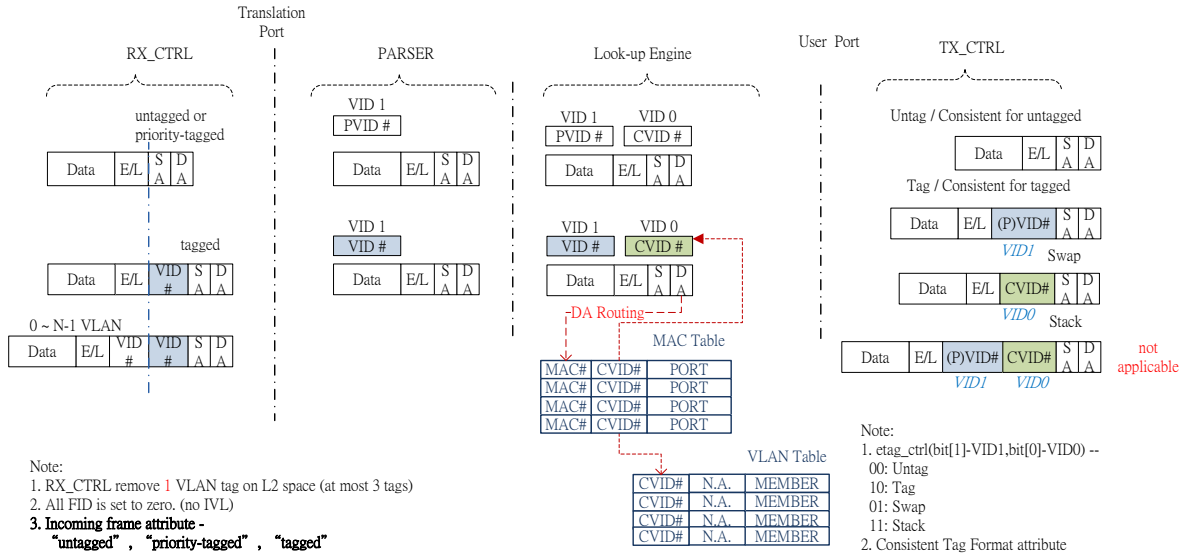



*VLAN Tag Process on User Port*

## Translation Port

The translation port is designated for 1:1 or N:1 VLAN aggregation according to CHINA TELECOM EPON requirement. When an incoming frame is received on the translation port, the corresponding custom VID will be found from MAC table, and then the CVID will be the VID for VLAN table.

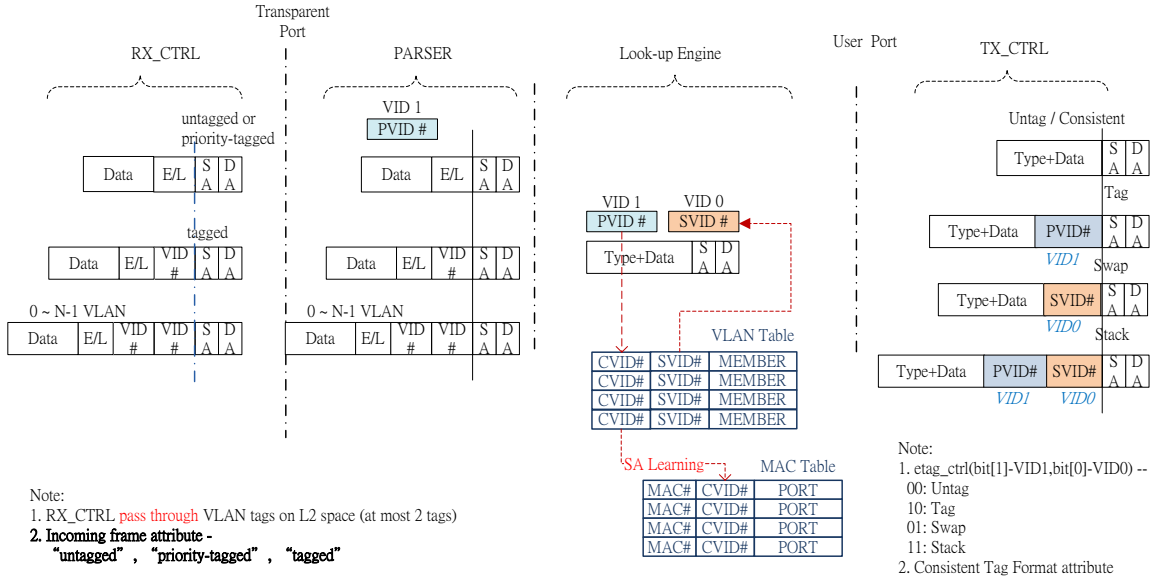
In the uploading direction, several custom VIDs can be translated into one service VID from the VLAN table which is carried on VID0. When this frame is transmitted from the translation port, etag_ctrl[1:0] will be 2'b01 (Swap), and the service VID will appear on the egress frame.




VLAN Tag Process on Translation Port

## Transparent Port

When the port is chosen as transparent port, the VLAN tags on the incoming will be ignored and treated as un-tagged frames. VID0 and VID1 will store PVID as the default VID which is used to look up the VLAN table. On the egress side, TX_CTRL can accept "UNTAG" control to send the original frame.




*VLAN Tag Process on Transparent Port*

## Security mode

Enable 802.1Q VLAN for all the received frames.
Discard received frame due to ingress membership violation (interrupt CPU)
Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

### Check mode

Enable 802.1Q function for all the received frames.
Don’t discard received frame due to ingress membership violation
Discard received frames once if VID is missed on the VLAN table (interrupt CPU)

### Fallback mode

Enable 802.1Q function for all the received frames.
Don’t discard received frame due to ingress membership violation
Frames whose VID is missed on the VLAN table will be filtered by the Port Matrix Member

### Port Matrix mode

802.1Q function disables (VLAN Security and VLAN Filter Table)
*Frames filtered by the Port Matrix Member*