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MT7612E DATASHEET

802.11a/b/g/n/ac Wi-Fi 2T2R Single Chip

Document Revision History

Revision	Date	Author	Description
0.01	2012/11/15	Ben Lin	Preliminary release
0.02	2012/11/27	Ben Lin	1. Correct the pin definition of pin 58 and pin 68. 2. Revise 2.4 IO control option.
0.03	2012/12/15	Ben Lin	1. Modify pin sequence of 74, 75, and 76. 2. Modify pin 40 LXBK description. 3. Correct Table 3: IO control option.
0.04	2013/4/3	Ben Lin	1. Modify pin 34, 55, 56 definition
0.90	2013/8/15	Ben Lin	1. Add section 3.6 Wi-Fi RF specification 2. Add section 3.7 PMU electrical characteristics 3. Add chapter 4 functional specification
1.00	2013/10/7	Ben Lin	1. Update power consumption. 2. Refine the description in section 2.3 and 2.4.
1.01	2013/11/25	Ben Lin	1. Add Wi-Fi RF specification for VHT20 part in section 3.6. 2. Correct the absolute maximum rate on VDD33 in section 3.1. 3. Correct the description of pin 12 and pin 13 in section 2.2.

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1 System Overview

1.1 General Descriptions

The MT7612E is a highly integrated single chip which has built in a 2x2 dual-band wireless LAN radio. It supports IEEE 802.11ac draft standard and provides the highest PHY rate up to 867Mbps, offering feature-rich wireless connectivity and reliable throughput from an extended distance.
Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. MT7612E integrates PA/LNA such that the number of the external components is reduced to minimum. Intelligent MAC design deploys a high efficient DMA engine and hardware data processing accelerators which offloads the host processor.
The MT7612E supports the 802.11i security standard and implements hardware acceleration for TKIP, CCMP and WAPI. The device also supports 802.11e QoS for video, voice, and multimedia applications.

1.2 Features

1.2.1 Platform

- Embedded high-performance 32-bit RISC microprocessor
- Highly integrated RF with 55nm CMOS technology
- Integrate high efficiency switching regulator
- 20/40MHz crystal clock support with low power operation in sleep mode
- Best-in-class active and idle power consumption performance
- Compact 9mm x 9mm QFN76L package
- Fully compliance with PCIe base specification v1.1 with OBFF, LTR ECN support
- Buffered clock output for co-clock with other SOC chipset
- Integrate EFUSE to eliminate the requirement for external EEPROM
- External serial flash support
- 14 programmable general purpose Input / Output
- 2 configurable LED pins
- Internal thermal sensor for temperature compensation and thermal protection.
- Self calibration

1.2.2 WLAN

- IEEE 802.11 a/b/g/n and 802.11ac draft compliant
- Support 20MHz, 40MHz, 80MHz in 5GHz band, and 20MHz, 40MHz bandwidth in 2.4GHz band
- Dual-band 2T2R mode with data rate up to 867Mbps
- Support 256QAM in 2.4GHz band
- Support STBC, LDPC, MRC, and transmit Beamforming
- Greenfield, mixed mode, legacy modes support
- Frame aggregation
- Integrated LNA, PA, and T/R switch.
- Optional external LNA and PA support.

- IEEE 802.11 d/e/h/i/k/r/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- 802.11 to 802.3 header translation offload
- Supports Wi-Fi Direct
- Per packet transmit power control
- Wake on WLAN
- Conforms to EN300328 V1.8.1 (2012.08) and EN301893 V1.7.1 (2012.06)

1.3 Applications

MT7612E is designed for PCI Express Full/Half Mini Card as well as Next Generation Form Factor (NGFF). It is suitable for the following applications.

- Desktop PC
- Laptop NB
- Tablet NB
- xDSL modem
- AP router

1.4 Block Diagram

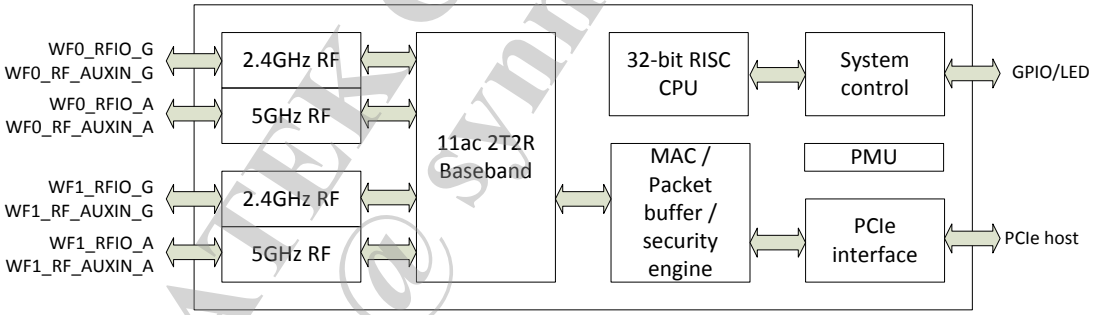


Figure 1 MT7612E block diagram

2 Product Descriptions

2.1 Pin Layout

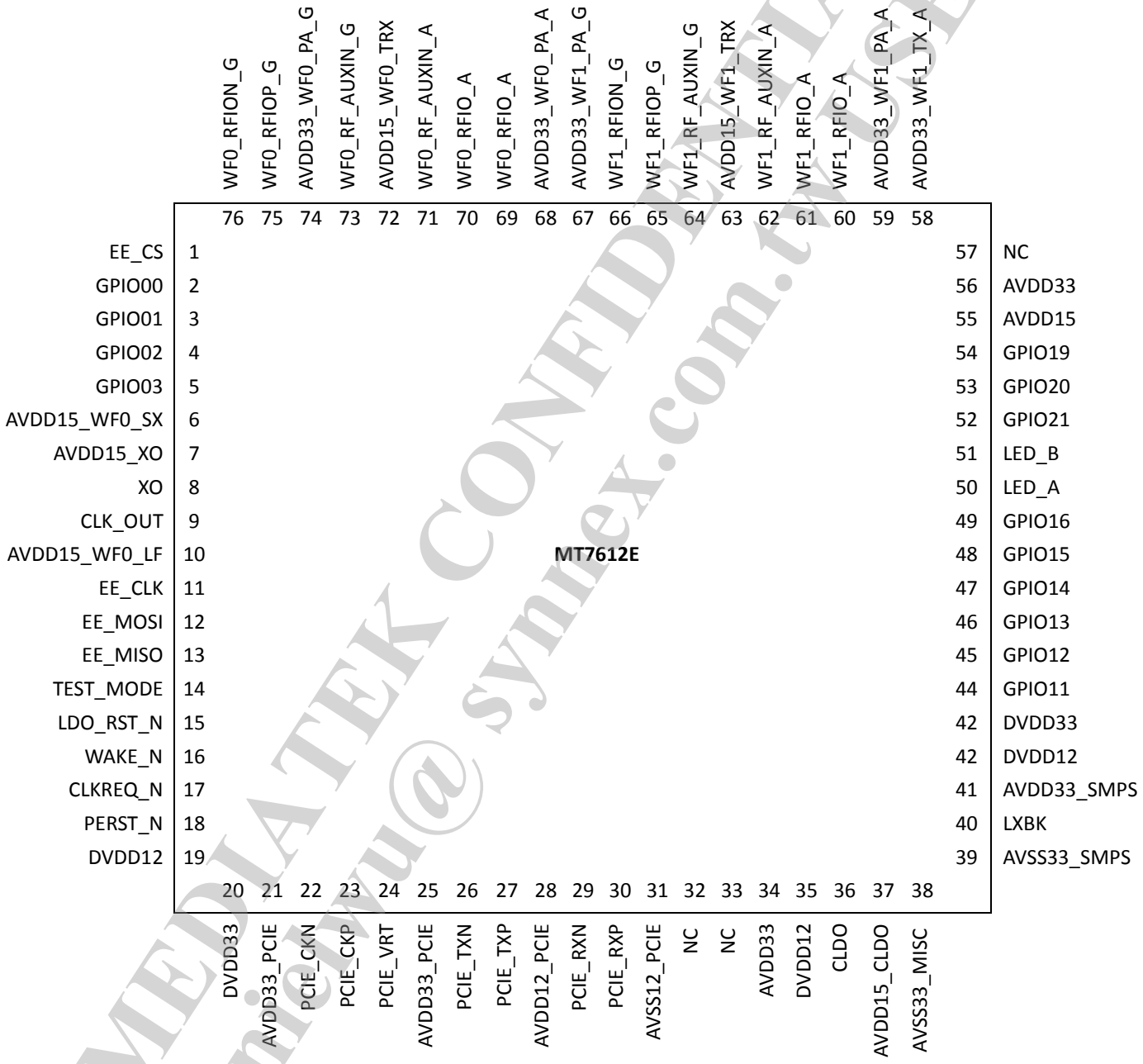


Figure 2 Top view of MT7612E QFN pin-out.

2.2 PIN Description

QFN76	Pin Name	Pin description	Default PU/PD	I/O	Supply domain
Reset and clocks					
15	LDO_RST_N	External system reset active low	N/A	Input	DVDD33
8	XO	Crystal input or external clock input	N/A	Input	AVDD15_XO
PCIe interface					
16	WAKE_N	Request system to wake from the sleep/suspend state	PU	Output	DVDD33
17	CLKREQ_N	Reference clock request signal	PU	Output	DVDD33
18	PERST_N	PCIe functional reset	PU	Input	DVDD33
22	PCIE_CKN	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
23	PCIE_CKP	PCIe differential reference clock	N/A	Input	AVDD33_PCIE
26	PCIE_TXN	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
27	PCIE_TXP	PCIe transmit differential pair	N/A	Output	AVDD33_PCIE
29	PCIE_RXN	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
30	PCIE_RXP	PCIe receive differential pair	N/A	Input	AVDD33_PCIE
24	PCIE_VRT	PCIe resister reference	N/A	Analog	
EEPROM/flash interface					
13	EE_MISO	External memory data input	PD	Input	DVDD33
12	EE_MOSI	External memory data output	PD	Output	DVDD33
11	EE_CLK	External clock	PD	Output	DVDD33
1	EE_CS	External chip select	PU	Output	DVDD33
Programmable I/O					
2	GPIO0	Programmable input/output	PD	In/out	DVDD33
3	GPIO1	Programmable input/output	PD	In/out	DVDD33
4	GPIO2	Programmable input/output	PD	In/out	DVDD33
5	GPIO3	Programmable input/output	PD	In/out	DVDD33
44	GPIO11	Programmable input/output	PD	In/out	DVDD33
45	GPIO12	Programmable input/output	PD	In/out	DVDD33
46	GPIO13	Programmable input/output	PD	In/out	DVDD33
47	GPIO14	Programmable input/output	PD	In/out	DVDD33
48	GPIO15	Programmable input/output	PD	In/out	DVDD33
49	GPIO16	Programmable input/output	PU	In/out	DVDD33

45	GPIO19	Programmable input/output	PD	In/out	DVDD33
53	GPIO20	Programmable input/output	PD	In/out	DVDD33
52	GPIO21	Programmable input/output	PD	In/out	DVDD33
LED					
50	LED_A	Programmable open-drain LED controller	PU	Output	DVDD33
51	LED_B	Programmable open-drain LED controller	PU	Output	DVDD33
WIFI radio interface					
60, 61	WF1_RFIO_A	RF a-band RF port	N/A	In/Out	
62	WF1_RF_AUXIN_A	RF a-band auxiliary RF LNA port	N/A	Input	
64	WF1_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Input	
65	WF1_RFIOP_G	RF g-band RF port	N/A	In/Out	
66	WF1_RFION_G	RF g-band RF port	N/A	In/Out	
69, 70	WF0_RFIO_A	RF a-band RF port	N/A	Input	
71	WF0_RF_AUXIN_A	RF a-band auxiliary RF LNA port	N/A	Input	
73	WF0_RF_AUXIN_G	RF g-band auxiliary RF LNA port	N/A	Input	
75	WF0_RFIOP_G	RF g-band RF port	N/A	In/Out	
76	WF0_RFION_G	RF g-band RF port	N/A	In/Out	
9	CLK_OUT	XTAL buffered clock output	N/A	Output	
PMU/SMPS					
36	CLDO	LDO 1.2V output	N/A	Output	
37	AVDD15_CLDO	Digital LDO 1.5V input	N/A	Input	
41	AVDD33_SMPS	SMPS 3.3V power supply	N/A	Input	
40	LXBK	SMPS 1.5V output	N/A	Output	
Miscellaneous					
14	TEST_MODE	Test mode enable	N/A	Input	DVDD33
Power supplies					
20, 43	DVDD33	Digital 3.3v I/O power supply	N/A	Power	
19, 35, 42	DVDD12	Digital 1.2v core power supply	N/A	Power	
21, 25	AVDD33_PCIE	PCIe 3.3V power supply	N/A	Power	
28	AVDD12_PCIE	PCIe 1.2V power supply	N/A	Power	
58	AVDD33_WF1_TX_A	RF 3.3v power supply	N/A	Power	
59	AVDD33_WF1_PA_A	RF 3.3v power supply	N/A	Power	
67	AVDD33_WF1_PA_G	RF 3.3v power supply	N/A	Power	
68	AVDD33_WF0_PA_A	RF 3.3v power supply	N/A	Power	
74	AVDD33_WF0_PA_G	RF 3.3v power supply	N/A	Power	
34, 56	AVDD33	Analog power supply	N/A	Power	

6	AVDD15_WF0_SX	RF 1.5v power supply	N/A	Power	
7	AVDD15_XO	RF 1.5v power supply	N/A	Power	
10	AVDD15_WF0_LF	RF 1.5v power supply	N/A	Power	
63	AVDD15_WF1_TRX	RF 1.5v power supply	N/A	Power	
72	AVDD15_WF0_TRX	RF 1.5v power supply	N/A	Power	
55	AVDD15	Analog 1.5v power supply	N/A	Power	
31	AVSS12_PCIE	PCIe ground	N/A	Ground	
38	AVSS33_MISC	PMU ground	N/A	Ground	
39	AVSS33_SMPS	PMU ground	N/A	Ground	
32, 33, 57	NC	Reserved	N/A	N/A	
E-PAD	VSS	Ground	N/A	Ground	

Table 1 Pin descriptions

2.3 Strapping option

5 pins are used to set the default status of the chip for different applications. The pins are all internally pulled down. The users can connect the pin with an external small resistor (1KΩ or less) to VDD33 when they want to change the application. Those pins are sampled at Power-On-reset to determine the default status.

EXT_EE_SEL is used to identify if the external EEPROM or the internal Efuse is used. XTAL_20_SEL is used to identify if 20MHz or 40MHz clock is used. CHIP_MODE is used for testing purpose, and the user should set normal mode for normal application.

QFN76	Pin Name	Pin description	Instruction for external circuit
12	EE_MOSI	EXT_EE_SEL	EEPROM: connect to VDD33 Efuse: Not connect (internal pull down)
11	EE_CLK	XTAL_20_SEL	XTAL is 20MHz: connect to VDD33 XTAL is 40MHz: Not connect (internal pull down)
47	GPIO14	CHIP_MODE[2]	Normal mode: Not connect (Internal pull down)
46	GPIO13	CHIP_MODE[1]	Normal mode: Not connect (Internal pull down)
45	GPIO12	CHIP_MODE[0]	Normal mode: connect to VDD33

Table 2 Strapping option

2.4 IO control option

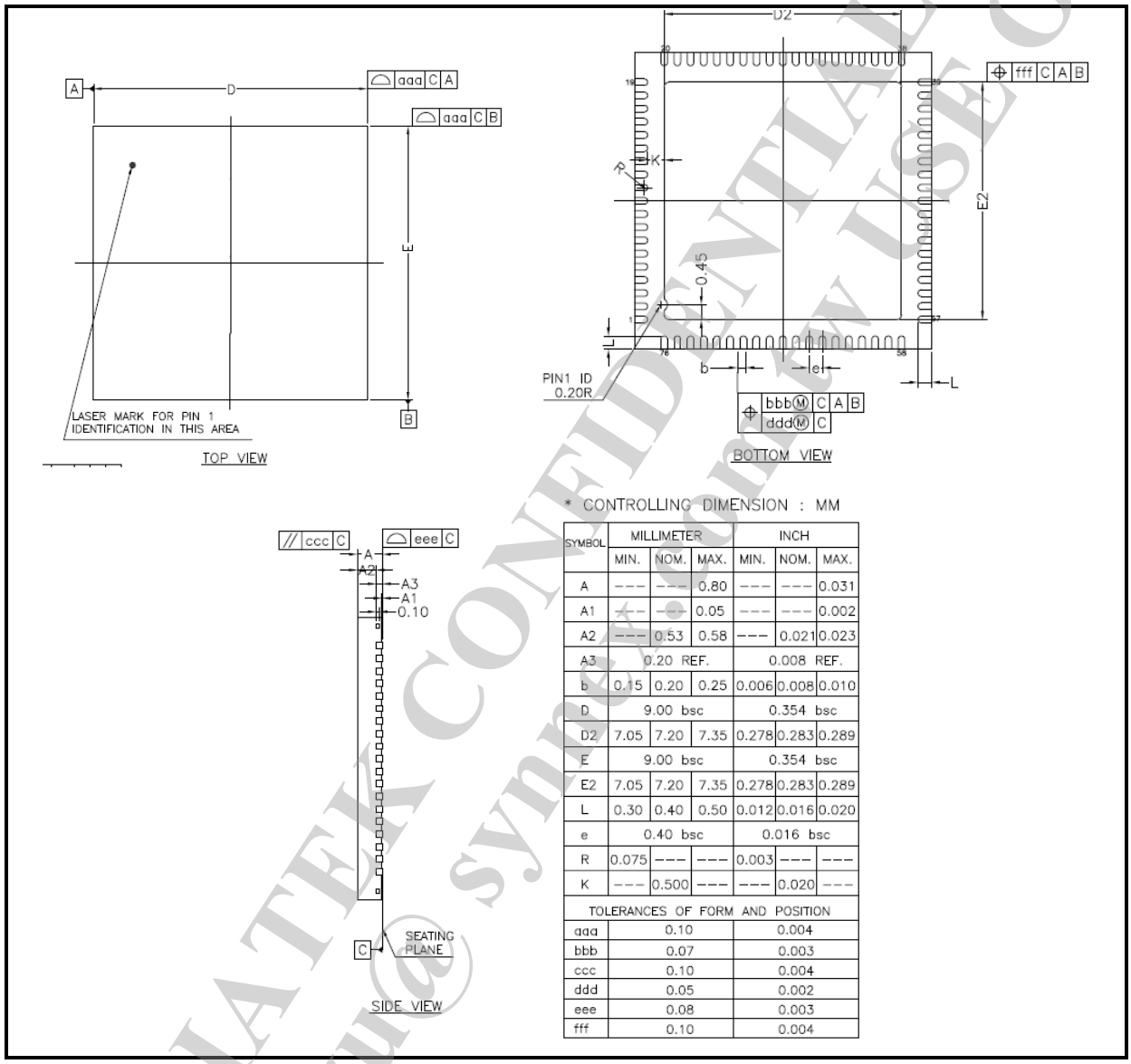
MT7612E provides 14 configurable I/O functions to support diversified applications. The IO functions can be configured through the control register IO_MODE. It supports external front-end module on dual bands for high power requirement. Open drained IOs are available for LED. The most common configuration is listed in the table below.

QFN76	Pin Name	GPIO mode	Default mode	IO mode 7	IO mode 4	IO mode 3
2	GPIO0	GPIO0	Reserved	Reserved	Reserved	Reserved
3	GPIO1	GPIO1	GPIO1	Reserved	GPIO1	Reserved

4	GPIO2	GPIO2	WL_DISABLE	Reserved	WL_DISABLE	WL_DISABLE
5	GPIO3	GPIO3	GPIO3	Reserved	GPIO3	Reserved
44	GPIO11	GPIO11	GPIO11	PA2G_PE1	Reserved	GPIO11
45	GPIO12	GPIO12	GPIO12	PA2G_PE0	Reserved	LED_WL
46	GPIO13	GPIO13	GPIO13	PG5G_PE1	LNA2G5G_PE1	PA2G_PE1
47	GPIO14	GPIO14	GPIO14	PA5G_PE0	LNA2G5G_PE0	PA2G_PE0
48	GPIO15	GPIO15	Reserved	LNA2G5G_PE1	Reserved	Reserved
49	GPIO16	GPIO16	Reserved	LNA2G5G_PE0	Reserved	Reserved
50	LED_A	GPIO17	LED_WL	GPIO17	LED_WL	LNA2G5G_PE1
51	LED_B	GPIO18	LED_B	LED_B	LED_B	LNA2G5G_PE0
54	GPIO19	GPIO19	GPIO19	TRSW_N	TRSW_N	TRSW_N
53	GPIO20	GPIO20	Reserved	TRSW_P	TRSW_P	TRSW_P

Table 3 IO control option

2.5 Package information



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.80	---	---	0.031
A1	---	---	0.05	---	---	0.002
A2	---	0.53	0.58	---	0.021	0.023
A3	0.20 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	9.00 bsc			0.354 bsc		
D2	7.05	7.20	7.35	0.278	0.283	0.289
E	9.00 bsc			0.354 bsc		
E2	7.05	7.20	7.35	0.278	0.283	0.289
L	0.30	0.40	0.50	0.012	0.016	0.020
e	0.40 bsc			0.016 bsc		
R	0.075	---	---	0.003	---	---
K	---	0.500	---	---	0.020	---

TOLERANCES OF FORM AND POSITION		
aaa	0.10	0.004
bbb	0.07	0.003
ccc	0.10	0.004
ddd	0.05	0.002
eee	0.08	0.003
fff	0.10	0.004

Figure 3 Package outline drawing

2.6 Ordering Information

Part number	Package	Operational temperature range
MT7612EN	9x9x0.8 mm 76-QFN	-10~70°C
MT7612IEN	9x9x0.8 mm 76-QFN	-40~80°C

Table 4 Ordering information

2.7 TOP Marking Information


```
MT7612EN : Part number
DDDD     : Date code
####     : Internal control code
BBBBBBB  : Lot number
```

Figure 4 Top marking

3 Electrical characteristics

3.1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
VDD12	1.2V Supply Voltage	-0.3 to 1.5	V
VDD15	1.5V Supply Voltage	-0.3 to 1.8	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	2000	V

Table 5 Absolute maximum ratings

3.2 Recommended operating range

Symbol	Rating	MIN	TYP	MAX	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
$T_{AMBIENT, MT7612EN}$	Ambient Temperature	-10	-	70	°C
$T_{AMBIENT, MT7612IEN}$	Ambient Temperature	-40	-	85	°C

Table 6 Recommended operating range

3.3 DC characteristics

Symbol	Parameter	Conditions	MIN	MAX	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.6	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{T-}	Schmitt Trigger Negative Going Threshold Voltage	LVTTL	0.68	1.36	V
V_{T+}	Schmitt Trigger Positive Going Threshold Voltage		1.36	1.7	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 1.6~14 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 1.6~14 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	KΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	KΩ

Table 7 DC description

3.4 Thermal characteristics

Symbol	Description	Performance	
		TYP	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	17.58	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	10.51	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	2	°C/W

Note:
[1] JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm

[2] 9mm x 9mm QFN76L package

Table 8 Thermal information

3.5 Current consumption

3.5.1 WLAN current consumption

Description	Performance	
	TYP	Unit
Sleep mode	4	mA
RX Active, HT40, MCS7	296	mA
RX Active, VHT80, MCS9	372	mA
RX Power saving, DTIM=1	65	mA
RX Listen	236	mA
TX HT40, MCS7 @15dBm	672	mA
TX VHT80, MCS9 @12dBm	772	mA
TX CCK, 11Mbps @19dBm	464	mA

Note: All result is measured with internal switching regulator enabled.

Table 9 WLAN Current Consumption

3.6 Wi-Fi RF specification

3.6.1 Wi-Fi RF Block Diagram

The frond-end loss with diplexer:

- 2.4GHz insertion loss is 0.8dB.
- 5GHz insertion loss is 1.7dB.

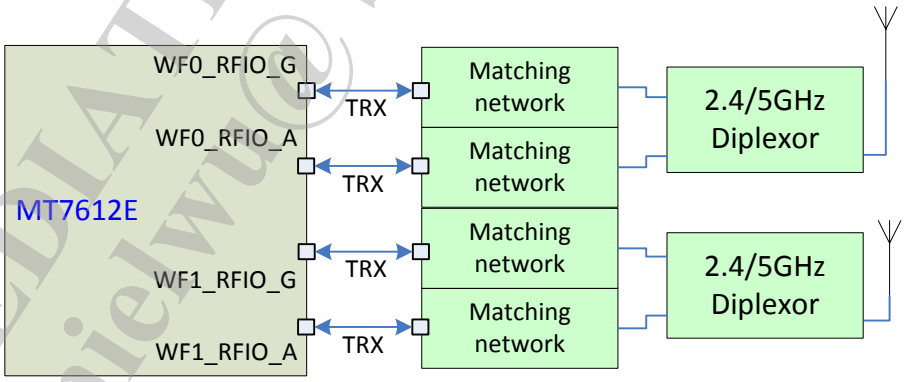


Figure 5 2.4/5GHz RF front-end configuration

3.6.2 Wi-Fi 2.4GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit

Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-98	-	dBm
	2 Mbps CCK	-	-94	-	dBm
	5.5 Mbps CCK	-	-92	-	dBm
	11 Mbps CCK	-	-89	-	dBm
RX sensitivity	6 Mbps OFDM	-	-92.5	-	dBm
	9 Mbps OFDM	-	-91.5	-	dBm
	12 Mbps OFDM	-	-91	-	dBm
	18 Mbps OFDM	-	-88.5	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-82	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-76	-	dBm
RX Sensitivity BW=20MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-92.5	-	dBm
	MCS 1	-	-89.5	-	dBm
	MCS 2	-	-88	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-81.5	-	dBm
	MCS 5	-	-77	-	dBm
	MCS 6	-	-75.5	-	dBm
	MCS 7	-	-74	-	dBm
RX Sensitivity BW=40MHz Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-89	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-84.5	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-74	-	dBm
	MCS 6	-	-72.5	-	dBm
	MCS 7	-	-71	-	dBm
Maximum Receive Level	11 Mbps CCK	-	-10	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	-	40	-	dBm
	11 Mbps CCK	-	36	-	dBm
	6 Mbps OFDM	-	39	-	dBm
	54 Mbps OFDM	-	22	-	dBm
Receive Adjacent Channel Rejection (HT20)	MCS 0	-	34	-	dBm
	MCS 7	-	9	-	dBm
Receive Adjacent Channel Rejection (HT40)	MCS 0	-	25	-	dBm
	MCS 7	-	9	-	dBm

Table 10 2.4GHz RF receiver specifications

3.6.3 Wi-Fi 2.4GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit

Frequency range		2412	-	2484	MHz
Output power	1~11 Mbps CCK	-	20	-	dBm
	6 Mbps OFDM	-	20	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20/HT40, MCS 0	-	20	-	dBm
	HT20/HT40, MCS 7	-	18	-	dBm
TSSI accuracy	Output power variation for close loop control	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Table 11 2.4GHz RF transmitter specifications

3.6.4 Wi-Fi 5GHz band RF receiver specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	GHz
RX sensitivity	6 Mbps OFDM	-	-91	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-89	-	dBm
	18 Mbps OFDM	-	-87.5	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	48 Mbps OFDM	-	-76.5	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX Sensitivity BW=20MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-91	-	dBm
	MCS 1	-	-89	-	dBm
	MCS 2	-	-87	-	dBm
	MCS 3	-	-83.5	-	dBm
	MCS 4	-	-81	-	dBm
	MCS 5	-	-75.5	-	dBm
	MCS 6	-	-74.5	-	dBm
	MCS 7	-	-73	-	dBm
	MCS 8	-	-68	-	dBm
RX Sensitivity BW=40MHz VHT Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-89	-	dBm
	MCS 1	-	-87	-	dBm
	MCS 2	-	-84.5	-	dBm
	MCS 3	-	-81	-	dBm
	MCS 4	-	-78	-	dBm
	MCS 5	-	-73.5	-	dBm
	MCS 6	-	-72	-	dBm
	MCS 7	-	-71	-	dBm
	MCS 8	-	-65	-	dBm
	MCS 9	-	-63.5	-	dBm
RX Sensitivity BW=80MHz VHT Green Field 800ns Guard Interval Non-STBC	MCS 0	-	-85	-	dBm
	MCS 1	-	-83.5	-	dBm
	MCS 2	-	-81	-	dBm
	MCS 3	-	-77.5	-	dBm
	MCS 4	-	-74	-	dBm
	MCS 5	-	-70	-	dBm

	MCS 6	-	-69	-	dBm
	MCS 7	-	-67	-	dBm
	MCS 8	-	-61.5	-	dBm
	MCS 9	-	-60	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection (VHT20)	MCS0	-	23	-	dBm
	MCS7	-	2	-	dBm
Receive Adjacent Channel Rejection (VHT40)	MCS 0	-	29	-	dBm
	MCS 7	-	5	-	dBm
Receive Adjacent Channel Rejection (VHT80)	MCS 0	-	26	-	dBm
	MCS 7	-	-3	-	dBm

Table 12 5GHz RF receiver specifications

3.6.5 Wi-Fi 5GHz band RF transmitter specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		MIN	TYP	MAX	Unit
Frequency range		5180	-	5825	MHz
Output power	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	15.5	-	dBm
	HT20/HT40, MCS 0	-	18	-	dBm
	HT20/HT40, MCS 7	-	15	-	dBm
	VHT80, MCS0	-	18	-	dBm
	VHT80, MCS9	-	14.5	-	dBm
Output Power Variation over RF frequency	TSSI accuracy	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Table 13 5GHz RF transmitter specifications

3.7 PMU electrical characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		MIN	TYP	MAX	Unit
Switching regulator					
Input voltage		2.97	3.3	3.63	V
Output voltage	Default voltage setting in the programmable range[1]	1.5	1.6	1.8	V
Output current		-	-	800	mA
Quiescent current	<1mA load current	-	40	55	uA
Line regulation	3V to 3.6V input voltage range @ no load	-	-	1	%

Load regulation	200mA to 600mA load current	-	-	0.05	mV/mA
Efficiency	300mA load current	-	85	-	%
Over-current Shutdown	Threshold	-	960	-	A
Digital LDO					
Input voltage		1.5	1.6	1.8	V
Output voltage		1.08	1.2	1.32	V
Output current		-	-	650	mA
Quiescent current		-	10	-	uA

Note 1: The programmable range of the output voltage of the switching regulator is 0.8V to 2.3V.

Table 14 PMU electrical characteristics

4 Functional specification

4.1 System

4.1.1 Power Management Unit

Power Management Unit (PMU) contains Low Drop-out Regulators (LDOs), highly efficient switching regulator, and the reference band-gap circuit. The circuits are optimized for quiescent current, drop-out voltage, line/load regulation, ripple rejection, and output noise.

Only one power source is required for MT7612E, The 3.3V power source is directly supplied to the switching regulator, digital I/Os, PCIe PHY, and RF related circuit. It's converted to 1.6V by the switching regulator for low voltage circuits. The built-in digital LDOs and RF LDOs converts 1.6V to 1.2V for digital, RF, PCIe PHY, and BBPLL core circuits.

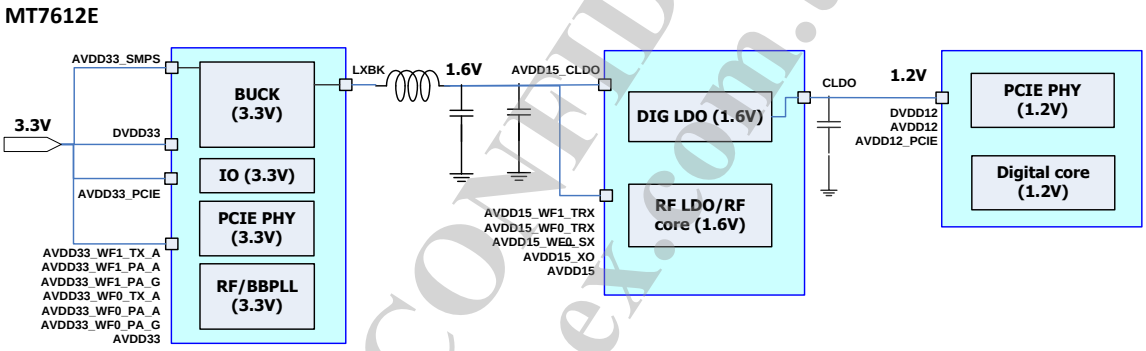


Figure 6 PMU block diagram

The switching regulator integrates the power MOS, and can provide 1A output current driving. It has output current limiting protection to prevent from circuit damage due to abnormal usage. It can reach 80% efficiency when operating at full loading. When the system operates in low power mode, it's turned off by the firmware to reduce the power consumption. It also has low noise spread spectrum operation to reduce the switching noise and the soft-start function.

4.1.2 EFUSE OTP

MT7612E uses embedded Efuse to store device specific configuration information such as MAC addresses, and power control settings.

Below illustrated the major fields defined in the Efuse.

- MAC addresses.
- Wi-Fi country code.
- TSSI parameters, TX power level.
- NIC configuration: RF front-end configuration, LED mode, baseband configuration.

4.1.3 GPIO

MT7612E has GPIO pins with software access. Pins are multiplexed with other functions including the LED control, External RF front-end module control, etc. Each GPIO support internal pull-up/pull-down options as well as driving strength control.

4.2 Host interface architecture

4.2.1 PCI Express

MT7612E supports the high-speed interface which conforms to the PCI Express Base Specification v1.1.
It supports PCIe link power states L0, L0s, L1, and L2. It also supports the new L1 sub-states with CLKREQ ECN as well the capability of Optimized Buffer Flush Fill (OBFF) and Latency Tolerance Reporting (LTR) to provide additional low power modes of operation.
The interface contains all necessary function blocks including transaction layer, data link layer, and physical layer. The standard configuration space and extended configuration space are supported.

4.3 MCU Subsystem

MCU subsystem contains the MCU, internal RAM/ROM and the ROM patch function.
MT7612E uses a 32-bit RISC MCU for low power consumption and efficient use of internal memory. The MCU controls the host interface, and controls the Wi-Fi hardware.

4.4 Wi-Fi Subsystem

4.4.1 Wi-Fi MAC

MT7612E MAC supports the following features:

- 802.11 to 802.3 header translation offload
- RX TCP/UDP/IP checksum offload
- Support multiple concurrent clients as an access point
- Support multiple concurrent clients as an repeater
- Shared TX and RX FIFO for maximum throughput
- Aggregate MPDU RX (de-aggregation) and TX (aggregation) support
- Aggregate MSDU support
- Beamforming
  - Explicit Beamforming with support of NDP and Stagger sounding
  - Explicit Beamforming with support of immediate feedback or delayed feedback generation using non-compressed and compressed steering matrix
  - Proprietary Implicit Beamforming using on-chip calibration.
- Transmit rate adaptation
- Transmit power control
- RTS with BW signaling
- CTS with BW signaling in response to RTS with BW signaling

- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing

4.4.2 WLAN Baseband

MT7612E baseband supports the following features:

- 11ac stage-1 feature support
  - 20, 40, and 80MHz channels
  - MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
  - MCS8-9 (256QAM, r=3/4 and r=5/6)
  - VHT A-MPDU delimiter for RX and TX for single MPDU
  - Clear Channel Assessment (CCA) on secondary
  - Short Guard Interval
  - STBC support
  - Low Density Parity check (LDPC) coding
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- Dynamic frequency selection (DFS) radar pulse detection

4.4.3 WLAN RF

MT7612E RF supports the following features:

- Integrated 2.4GHz/5GHz PA and LNA
- Integrated 5GHz Balun
- Support 2.4GHz/5GHz external PA and LNA

ESD CAUTION

MT7612E is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7632U is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.