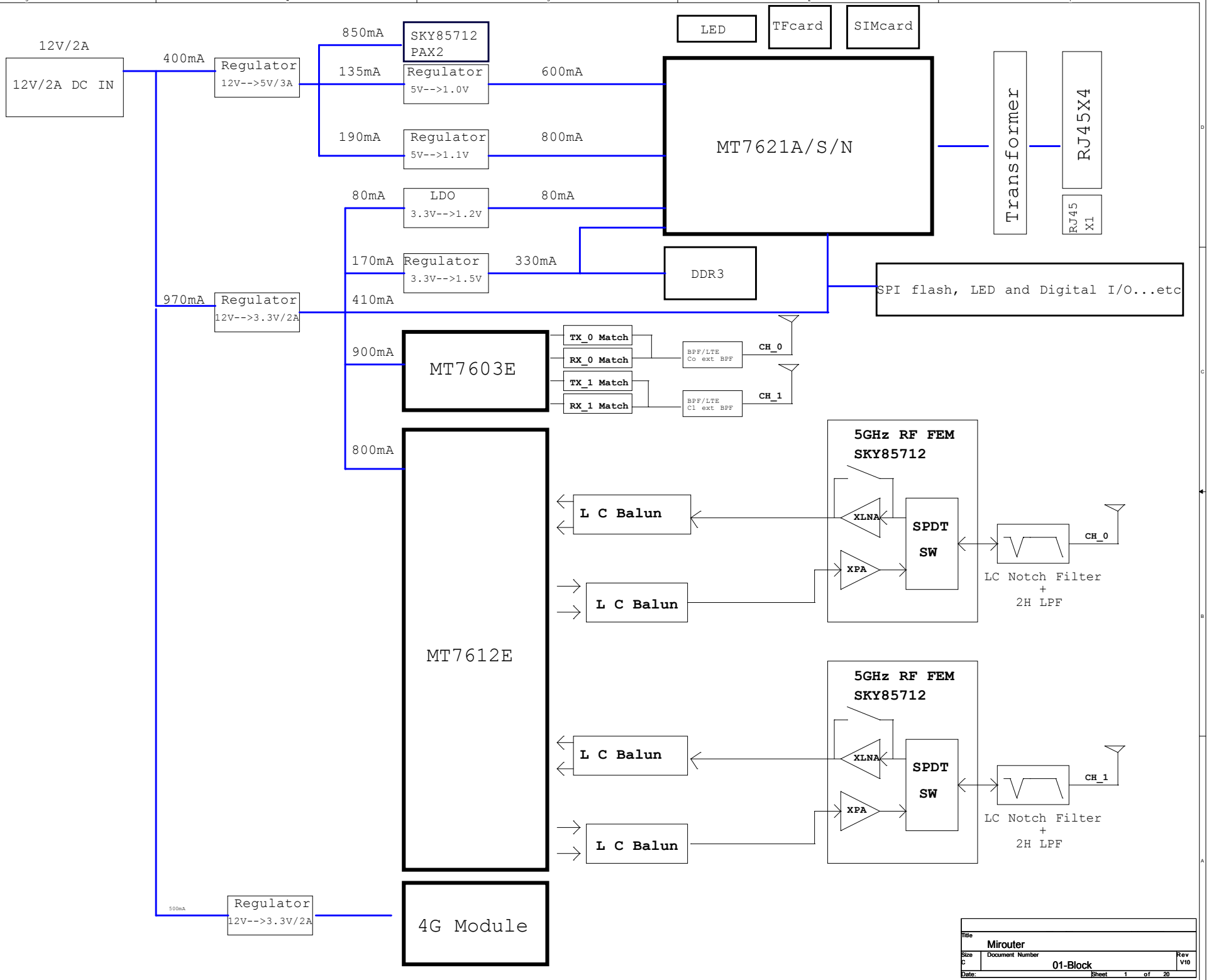
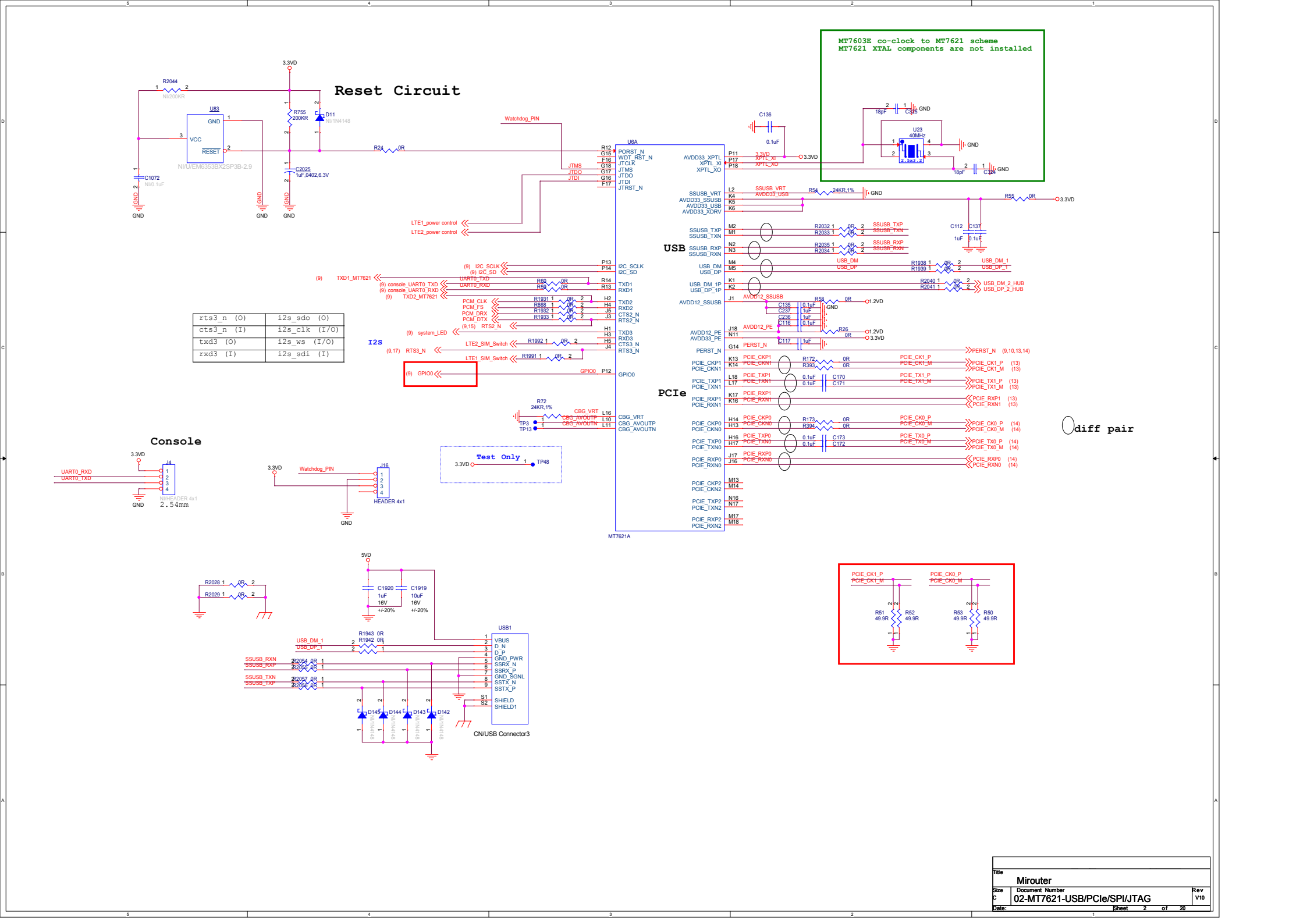

12V/2A
12V/2A DC IN
400mA
Regulator
12V-->5V/3A
850mA
SKY85712
PAX2
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
970mA
Regulator
12V-->3.3V/2A
410mA
500mA
Regulator
12V-->3.3V/2A
LED
TFcard
SIMcard
MT7621A/S/N
Transformer
RJ45X4
RJ45
X1
DDR3
SPI flash, LED and Digital I/O...etc
MT7603E
TX_0 Match
RX_0 Match
TX_1 Match
RX_1 Match
BPF/LTE
Co ext BPF
BPF/LTE
C1 ext BPF
CH_0
CH_1
900mA
MT7612E
800mA
5GHz RF FEM
SKY85712
L C Balun
L C Balun
XLNA
XPA
SPDT
SW
CH_0
LC Notch Filter
+
2H LPF
5GHz RF FEM
SKY85712
L C Balun
L C Balun
XLNA
XPA
SPDT
SW
CH_1
LC Notch Filter
+
2H LPF
4G Module
Title
Mirouter
Size
C
Document Number
01-Block
Rev
V10
Date:
Sheet 1 of 20



Title	Mirouter
Size C	Document Number 02-MT7621-USB/PCIe/SPI/JTAG
Rev	V10
Date:	Sheet 2 of 20

DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2

diff pair

Test Pad for signal measurement

(8) RDQ[0:15]

U6B

MT7621A

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

Nand Flash/ SD-XC/SPI Flash

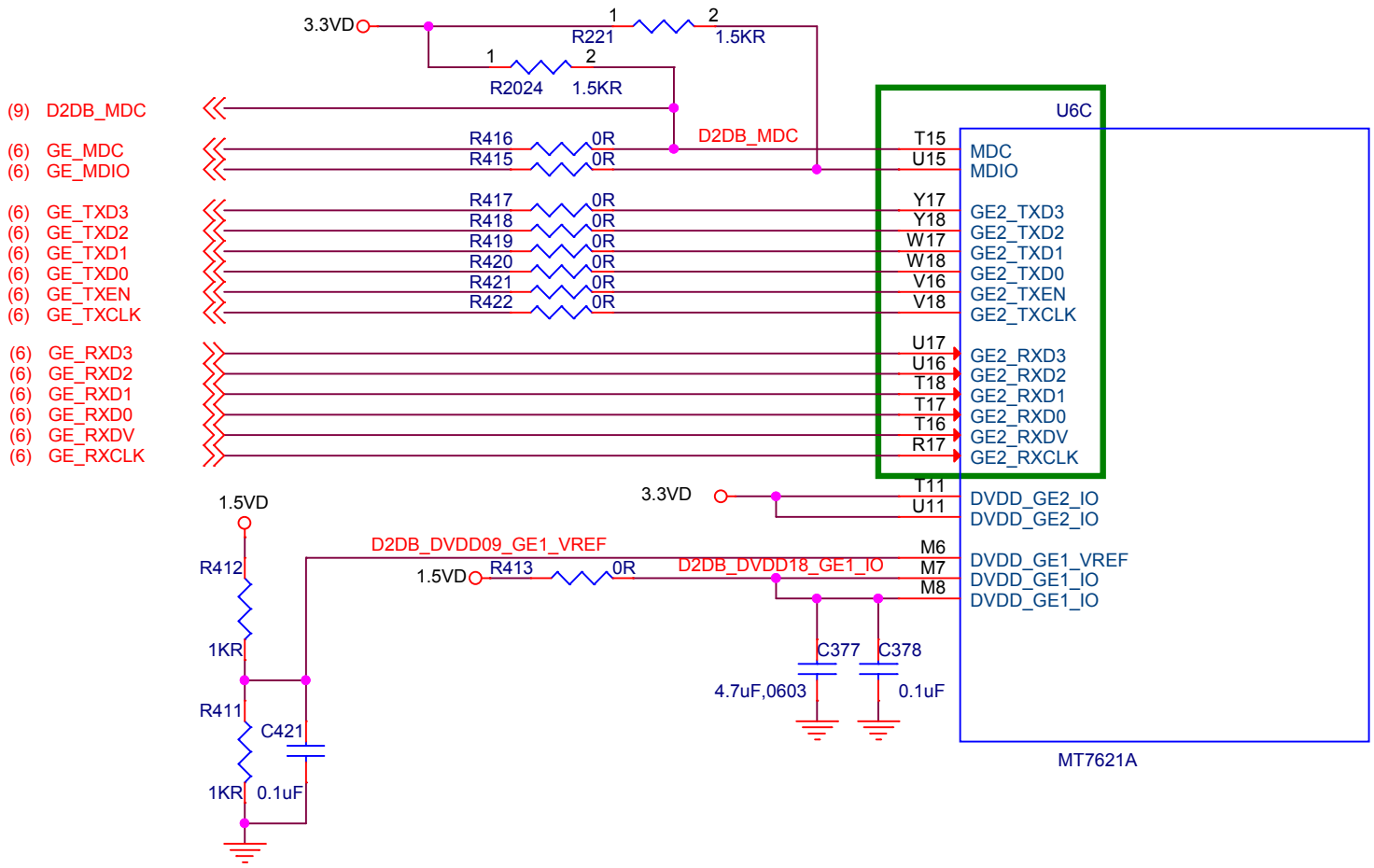
SPI Flash

W25Q128FVSF131B/MX25L25645GM21-08G

256Mbit Flash,W25Q256JV

Title	Mirouter
Size: B	Document Number: 03-MT7621-DDR3/NAND
Rev: V10	
Date:	Sheet 3 of 20

RGMII Interface

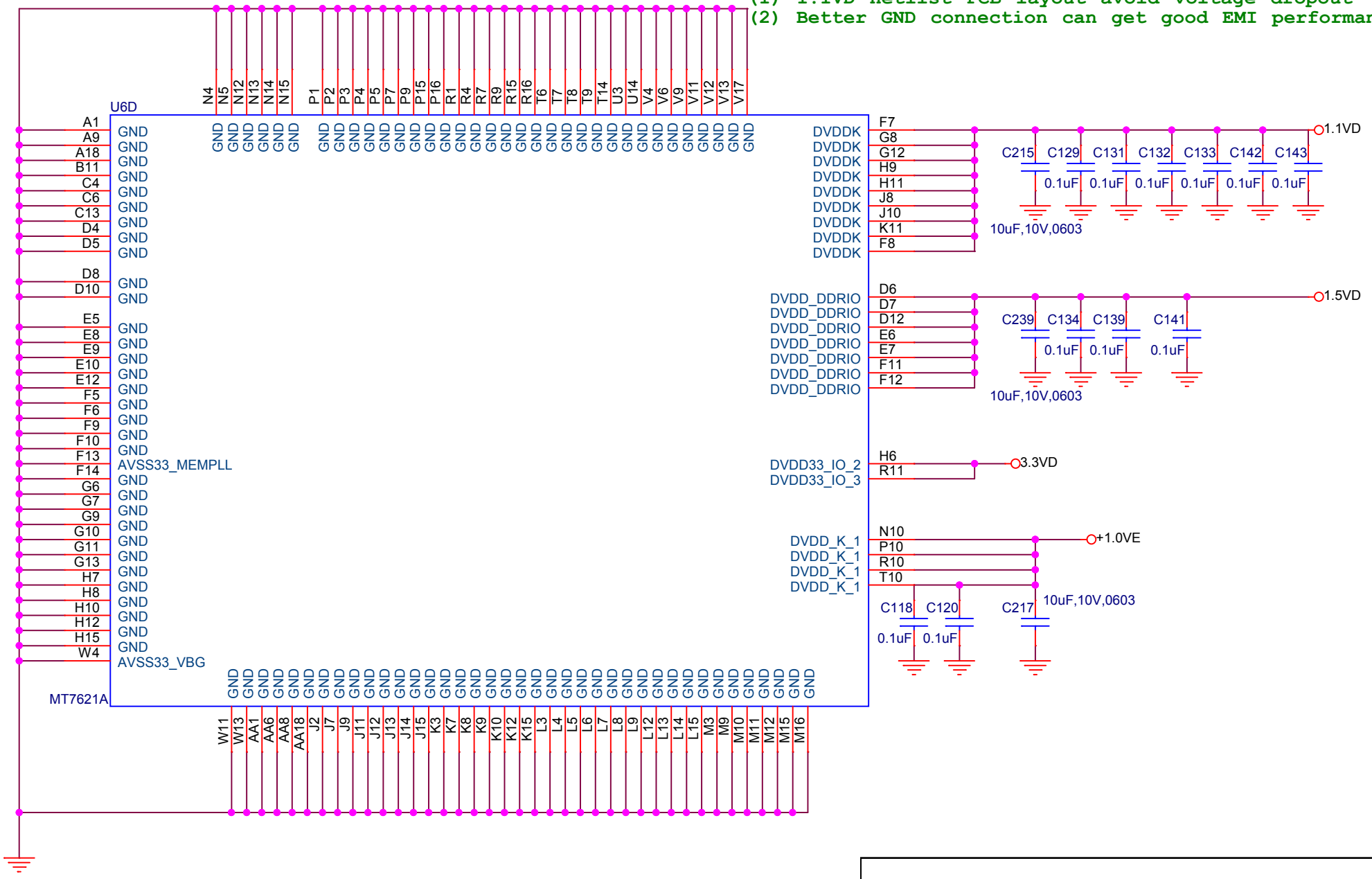


Note:
1. MT7621A/S MDC/MDIO cannot use to GPIO when needs control external/internal PHY
2. GE2 group cannot use to GPIO when WAN/LAN total bandwidth is up to 2G. Keeps the pin floating.

Title: Mirouter		
Size: A	Document Number: 04-MT7621-RGMII-EPHY	Rev: V10
Date:	Sheet 4 of 20	

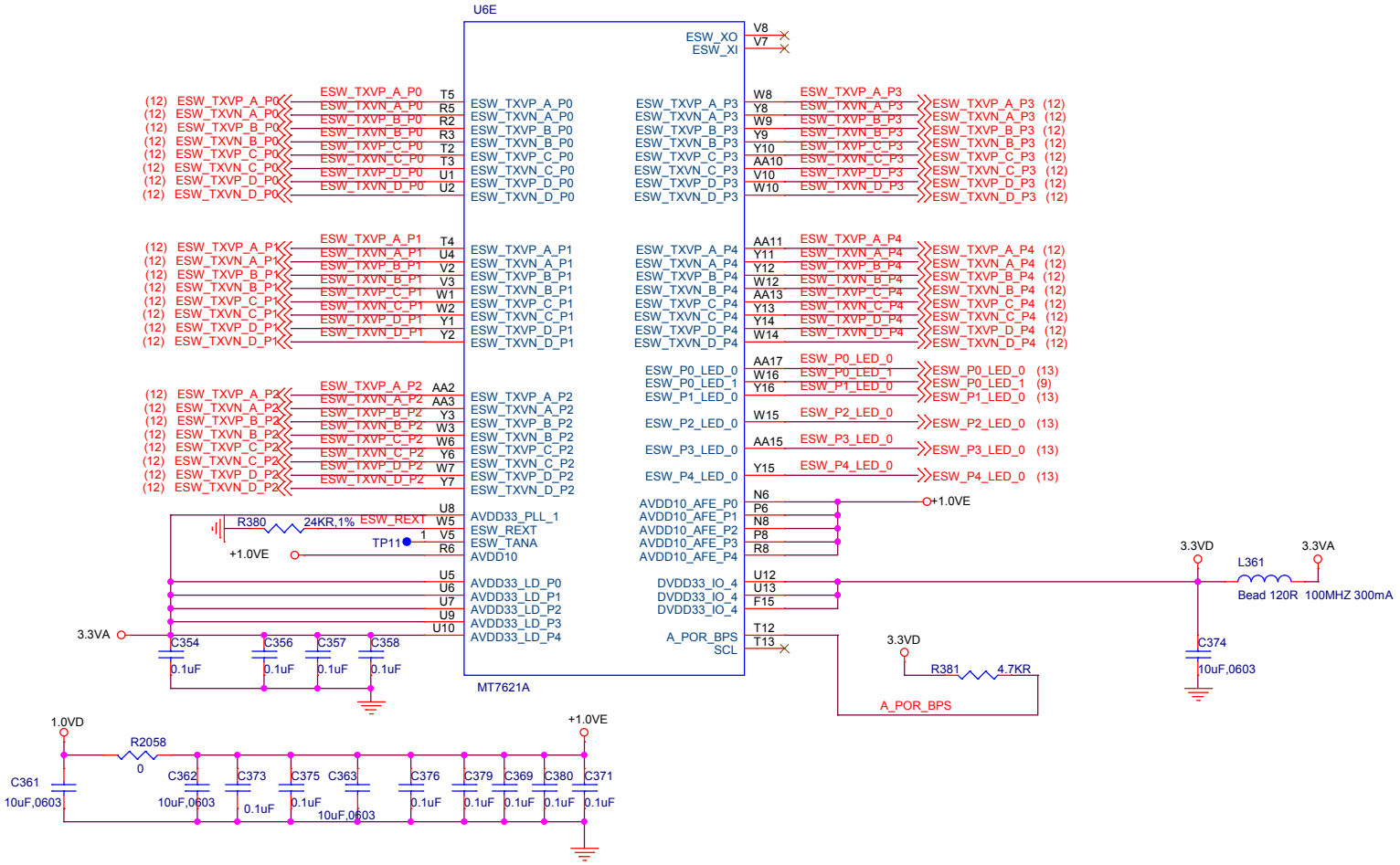
MT7621 Power

Please notice
Power and GND PCB layout is very important
(1) 1.1VD netlist PCB layout avoid voltage dropout
(2) Better GND connection can get good EMI performance

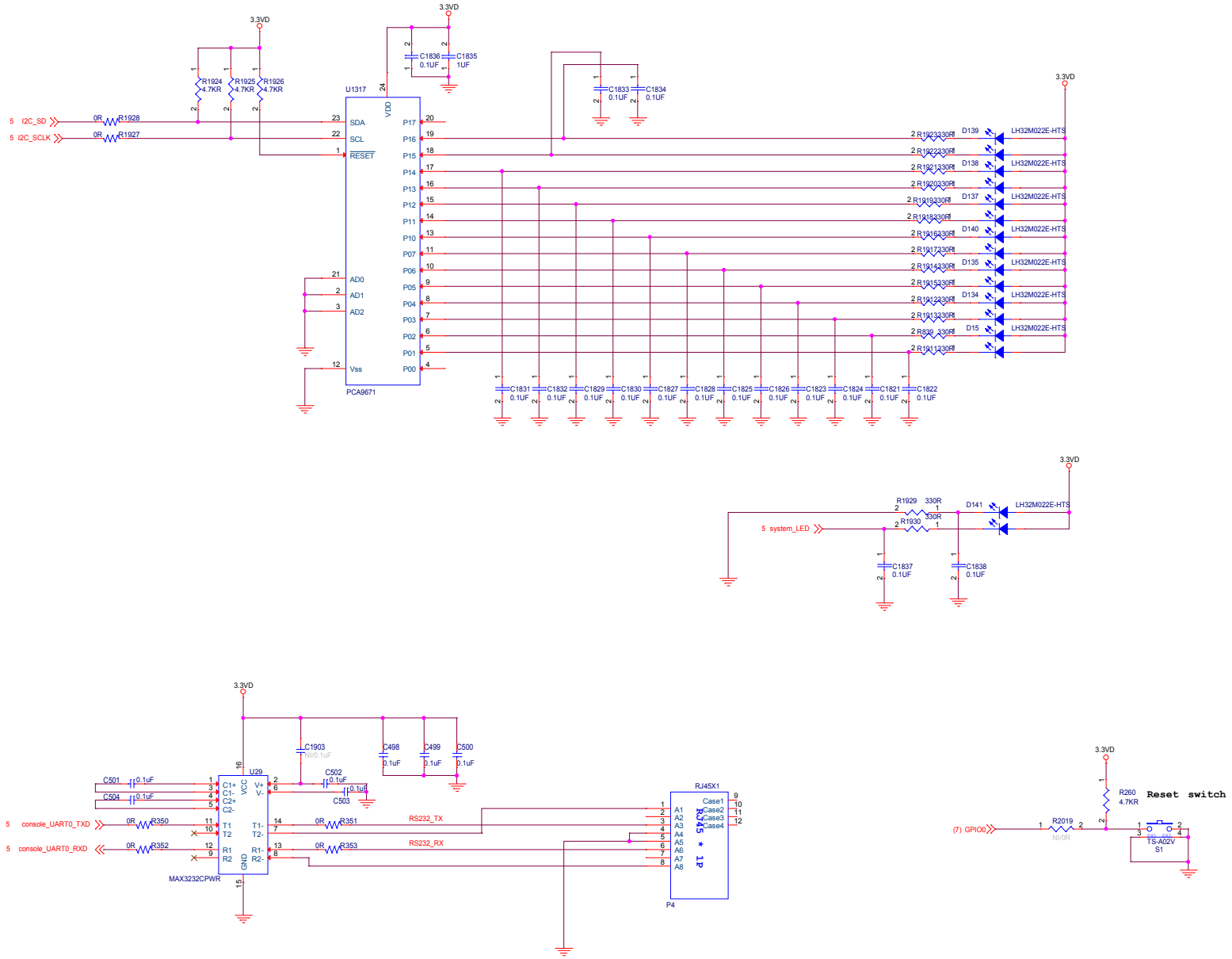


Title: Mirouter		
Size: A	Document Number: 05-MT7621-Power	Rev: V10
Date:	Sheet 5 of 20	

Giga SW

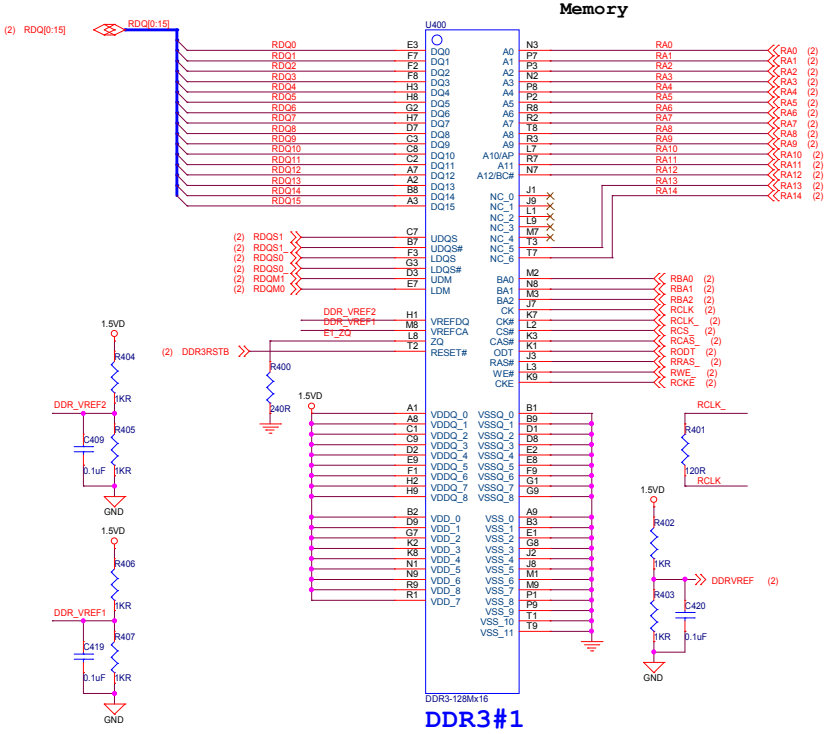


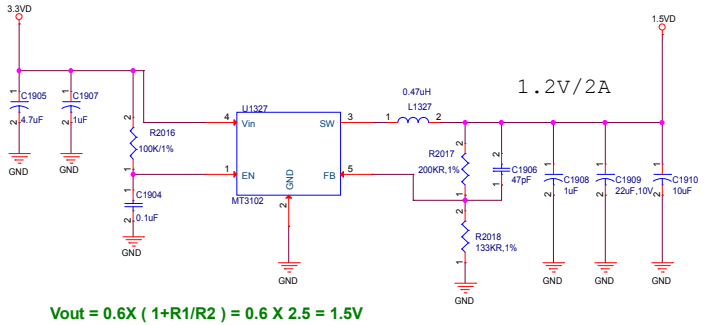
Title	Mirouter	
Size: B	Document Number: 06-MT7621-GbE I/F	Rev: V10
Date:	Sheet 6 of 20	



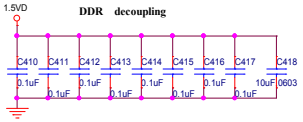
Title	Mirouter	
Size C	Document Number 07-LED	Rev V10
Date:	Sheet 7 of 20	

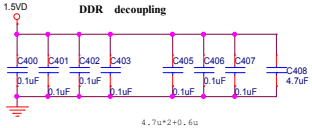
Memory

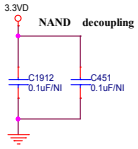




Vout = 0.6X (1+R1/R2) = 0.6 X 2.5 = 1.5V







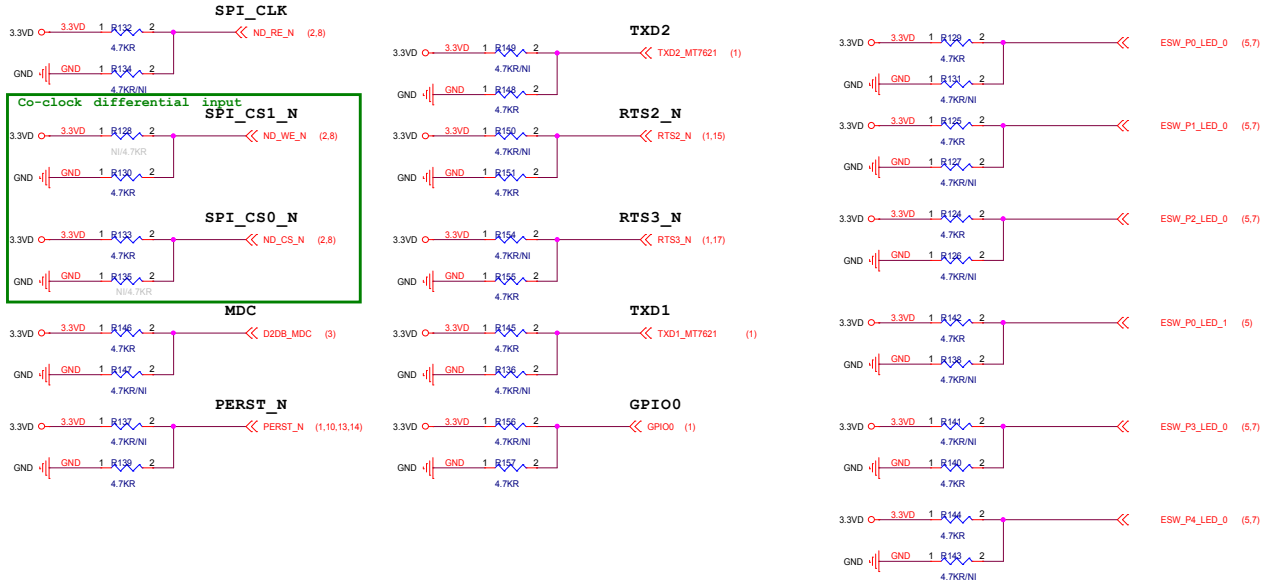
Title: Mirouter		
Size: C	Document Number: 08-MEM DDR3/NAND FLASH	Rev: V10
Date:	Sheet 8 of 20	

Boot Strapping

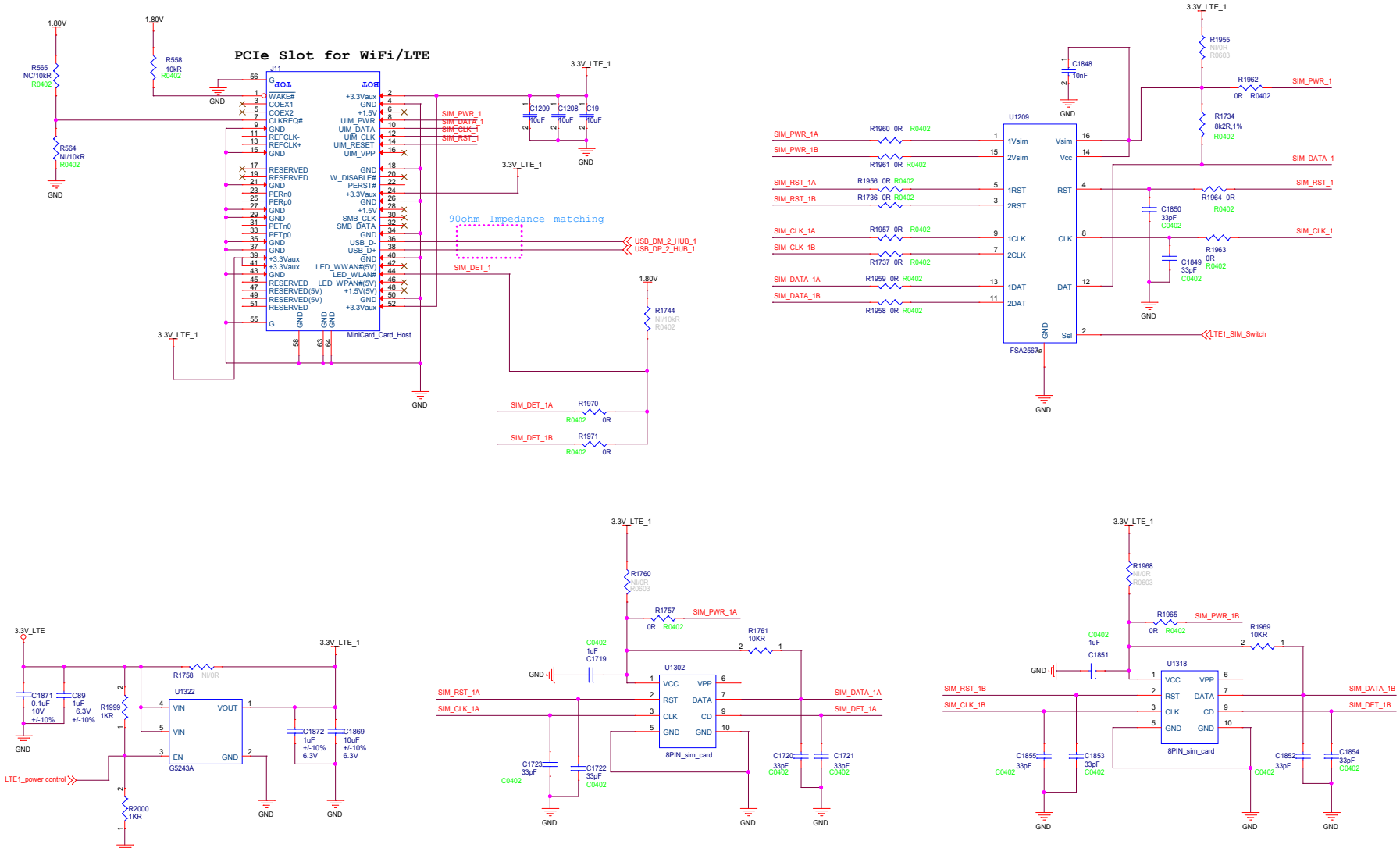
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	**011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input **101: 40 MHz, differential input** 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

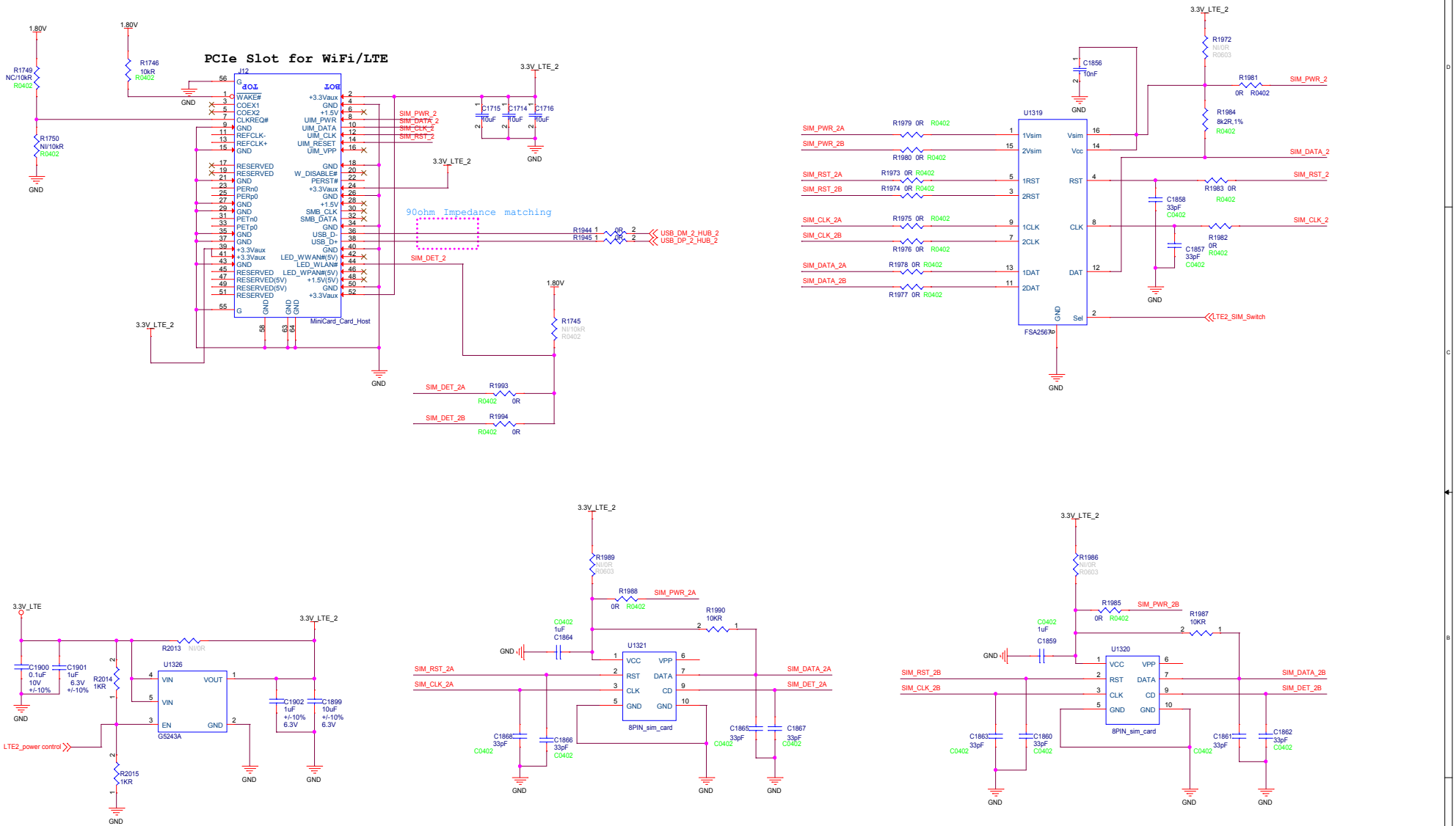
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



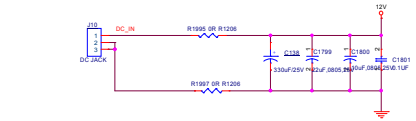
Title	Mirouter	
Size: C	Document Number: 09-Config	Rev: V10
Date:	Sheet 9 of 20	

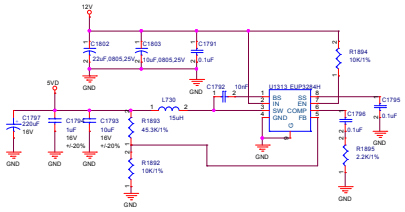


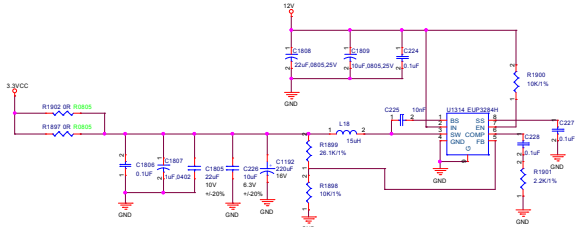
Title	Mirouter	
Size C	Document Number 10-PCIe Slot	Rev V10
Date:	Sheet 10 of 20	

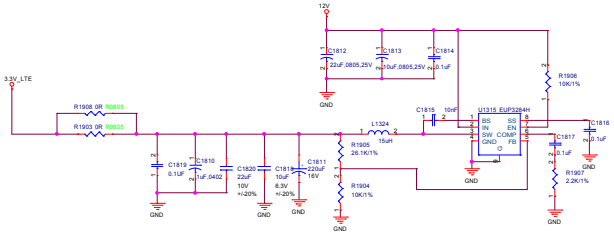


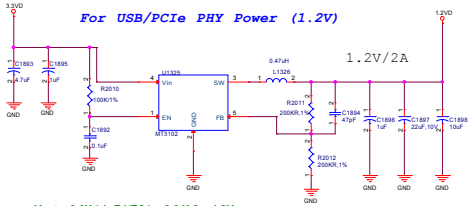
Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 11 of 20	



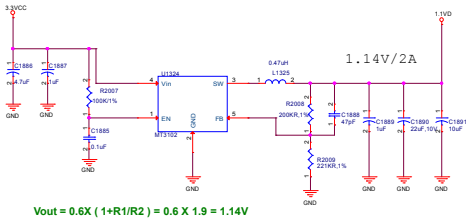




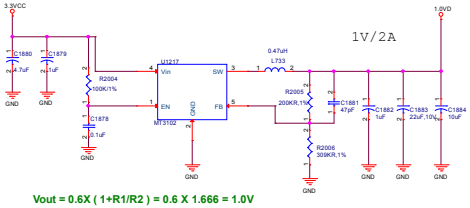




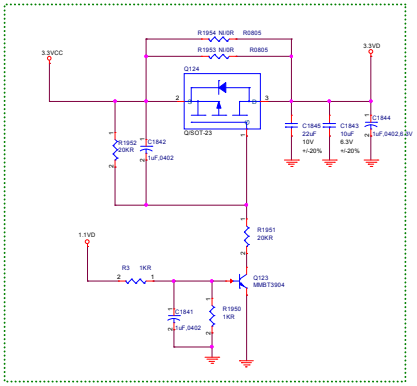
Vout = 0.6X (1+R1/R2) = 0.6 X 2 = 1.2V



Vout = 0.6X (1+R1/R2) = 0.6 X 1.9 = 1.14V



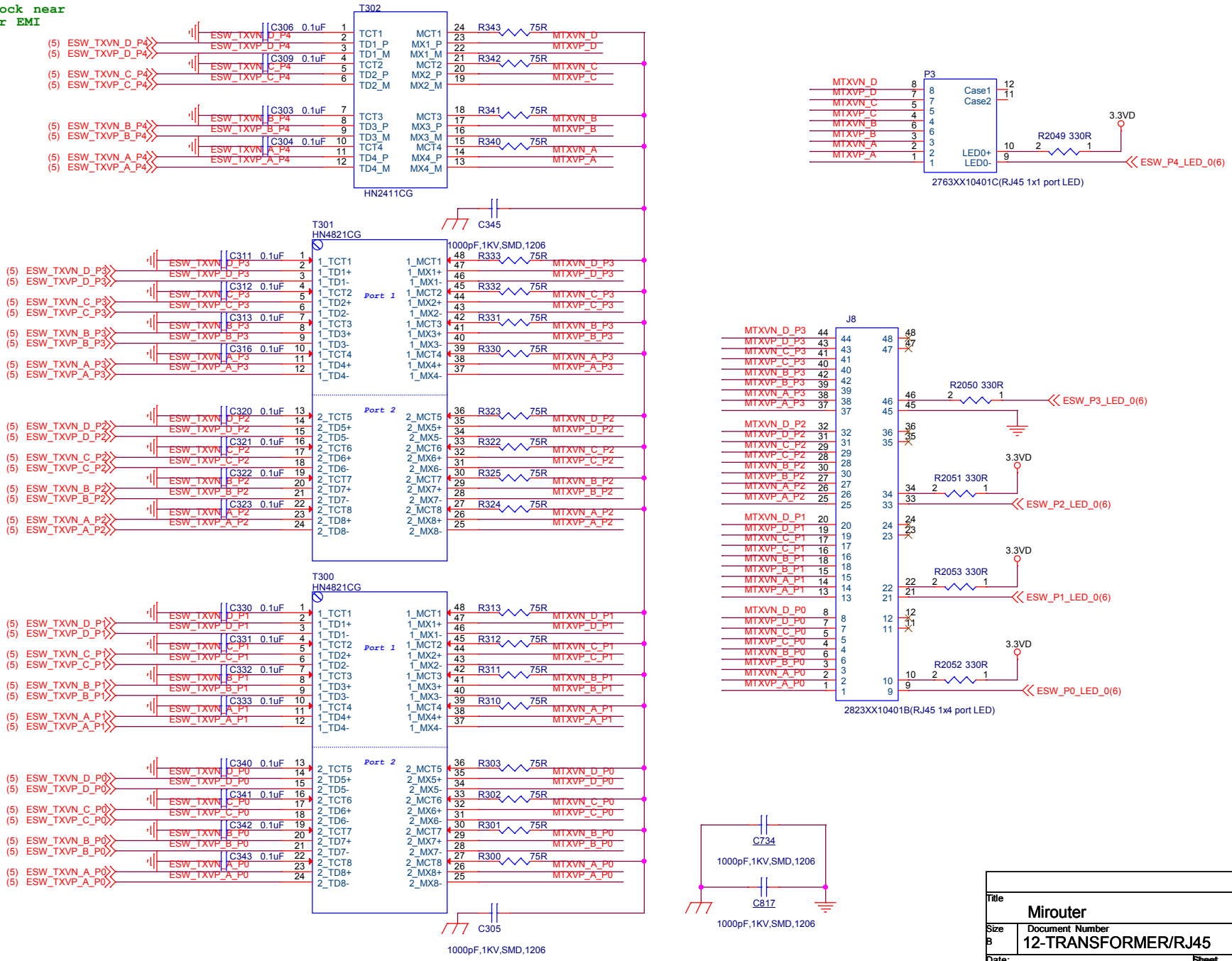
Vout = 0.6X (1+R1/R2) = 0.6 X 1.666 = 1.0V



for power on sequence

Title	Mirouter	
Size: D	Document Number: 11-POWER	Rev: V10
Date:	Sheet 12 of 20	

XMER choose common chock near
MT7621 side for better EMI



Title	Mirouter
Size	B
Document Number	12-TRANSFORMER/RJ45
Rev	V10
Date:	Sheet 13 of 20

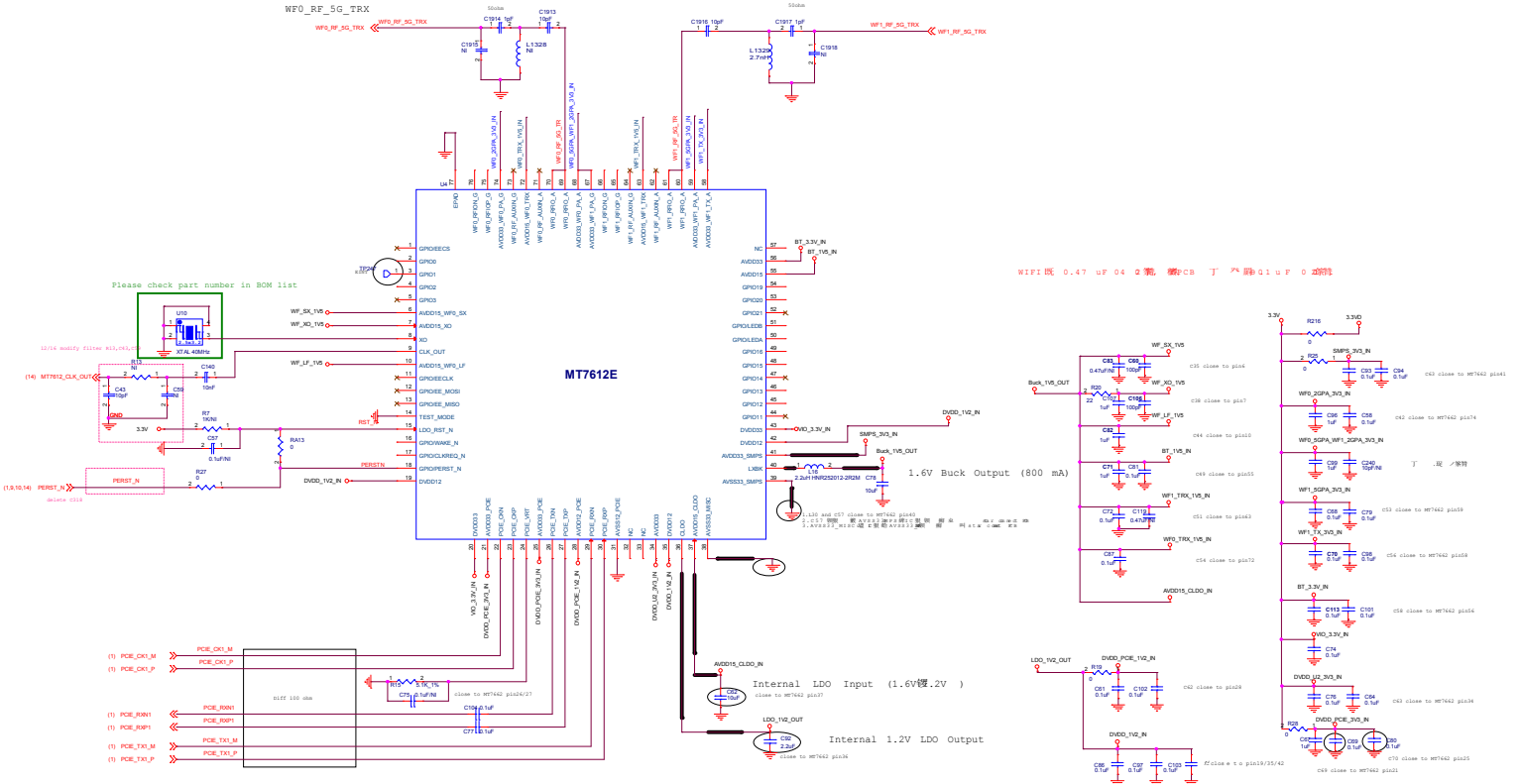
RF port is more sensitive to ESD for advanced silicon process.
The design of ESD protection must take into consideration since sample pilot run stage.
For detail, please contact with MTK technical contact window.

Place DC block capacitor near MT7612 RX pin. (red circle 1)

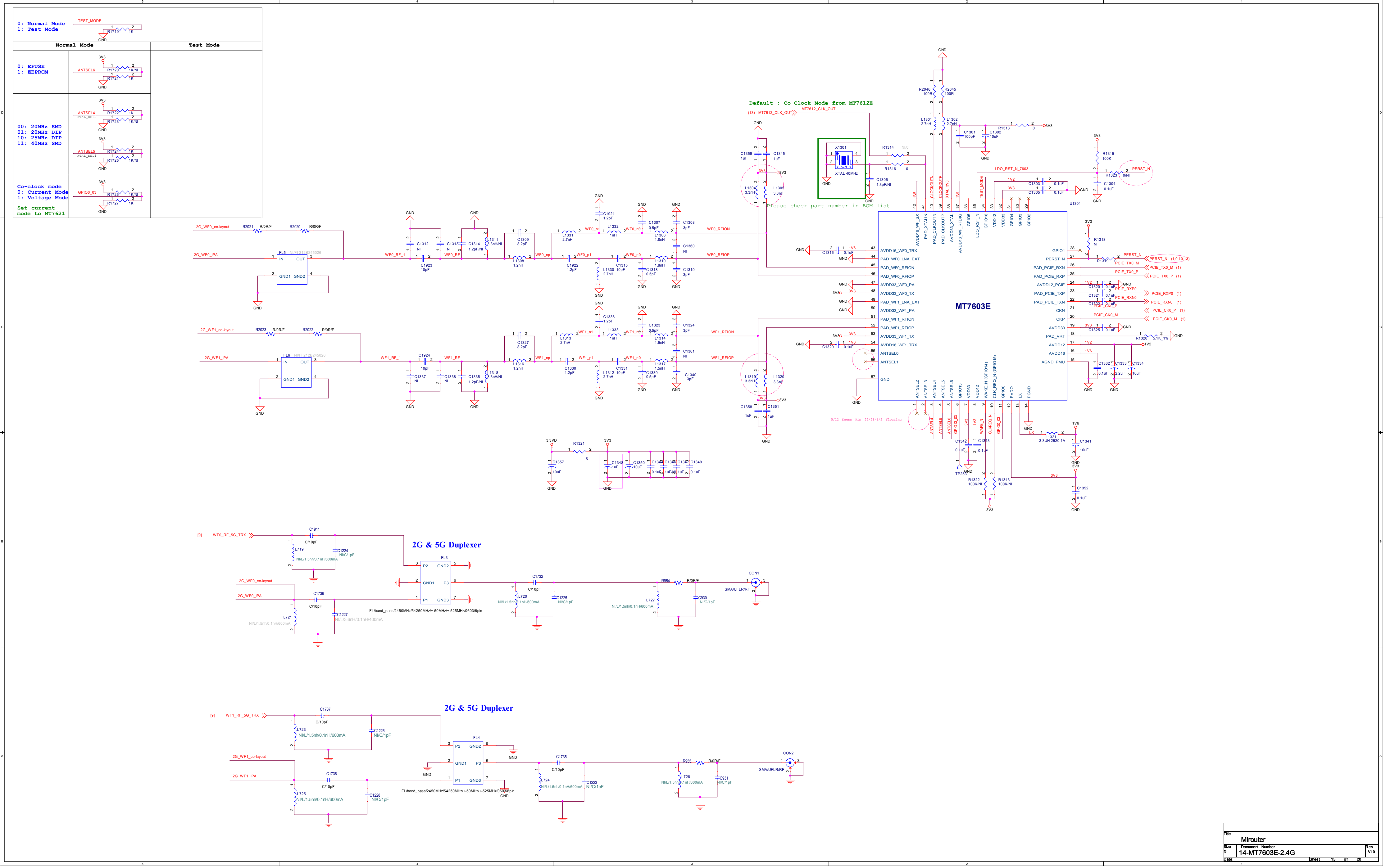
* If FEM has DC-block-capacitor inside design, system could use FEM component as ESD discharging path directly. For example, use C207,C242 0R instead of 10pF in SKY85601 case.(red circle 2)

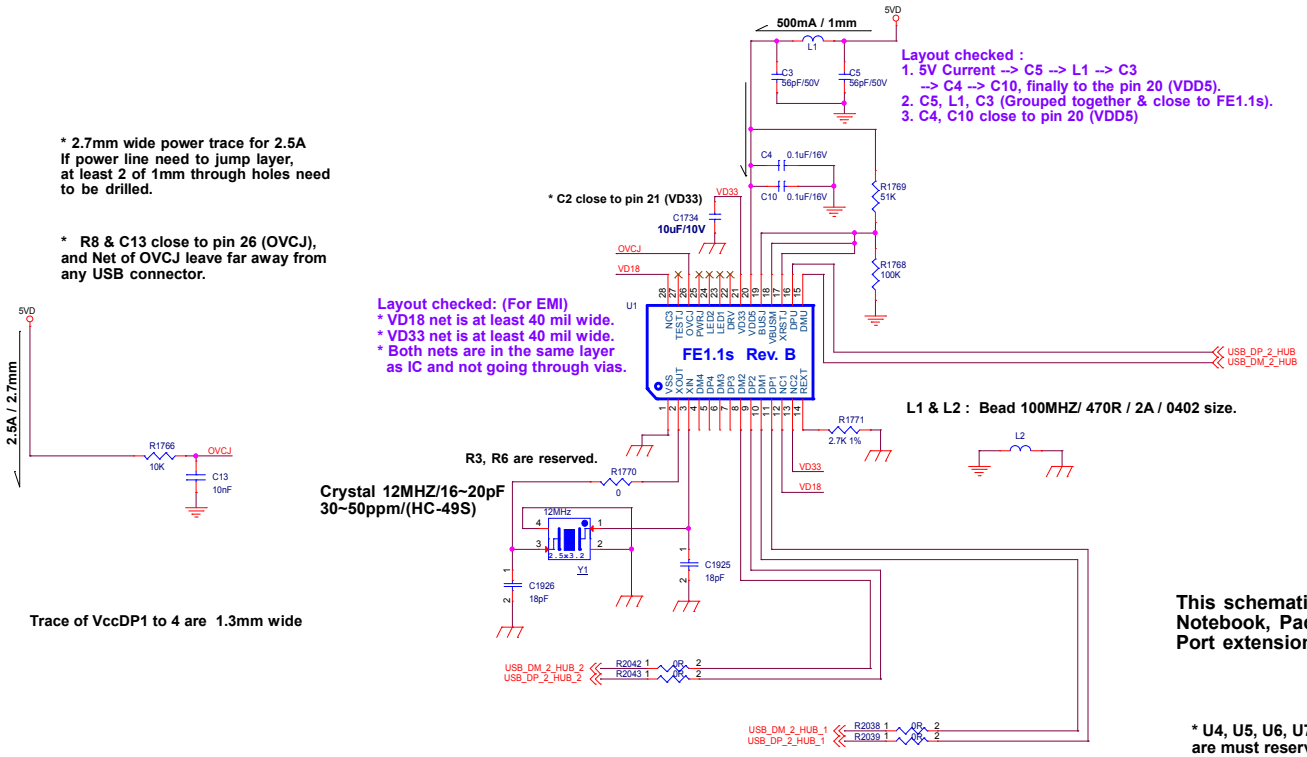
* Place MT7612E , DC block capacitor and FEM insides shielding case to avoid human touching.

Placement Note
C85 and C88 DC coupling capacitor should place in shielding case, and near MT7612E pin out

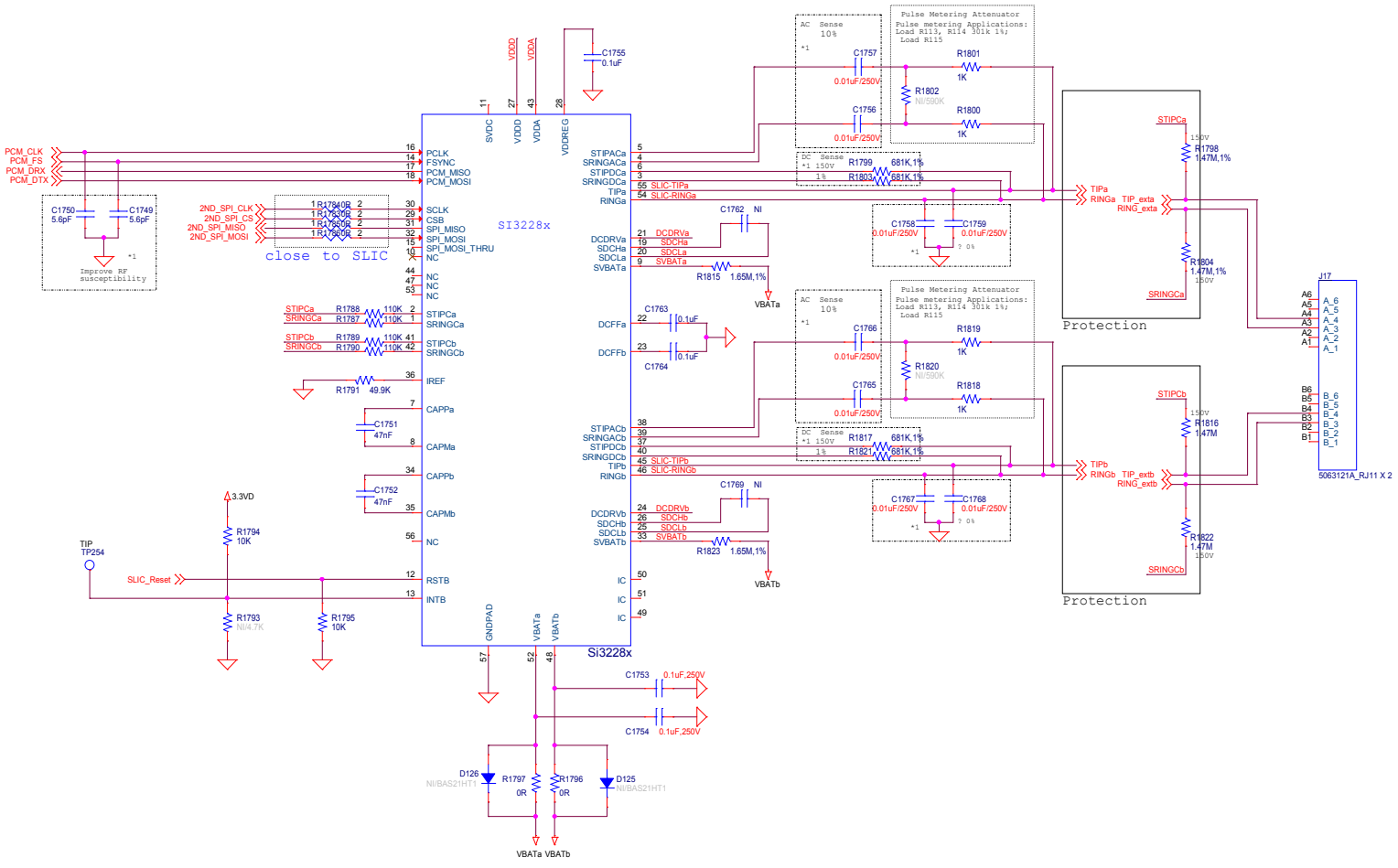


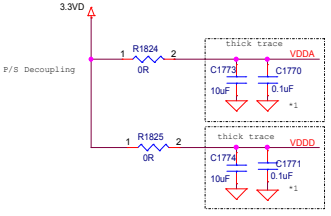
Mirouter		
Size	Document Number	Rev
Custom	13-MT7612E-5G	V10
Date:	Sheet 14 of 20	

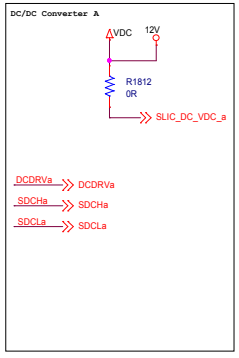

0: Normal Mode
1: Test Mode
TEST_MODE
Normal Mode
Test Mode
0: EFUSE
1: EEPROM
00: 20MHz SMD
01: 20MHz DIP
10: 25MHz DIP
11: 40MHz SMD
Co-clock mode
0: Current Mode
1: Voltage Mode
Set current mode to MT7621
Default : Co-Clock Mode from MT7612E
MT7612_CLK_OUT
XTAL 40MHz
Please check part number in BOM list
MT7603E
U1301
2G_WF0_co-layout
2G_WF0_iPA
2G_WF1_co-layout
2G_WF1_iPA
WF0_RFION
WF0_RFIOP
WF1_RFION
WF1_RFIOP
PERST_N
PCIE_TX0_M
PCIE_TX0_P
PCIE_RXP0
PCIE_RXN0
PCIE_CK0_P
PCIE_CK0_M
LDO_RST_N_7603
5/11 Keeps Pin 55/56/1/2 floating
2G & 5G Duplexer
WF0_RF_5G_TRX
WF1_RF_5G_TRX
FL/band_pass/2450MHz/54250MHz/+-50MHz/+-525MHz/0603/6pin
SMA/UFLR/RF
CON1
CON2
FL3
FL4
Title
Mirouter
Document Number
14-MT7603E-2.4G
Rev
V10
Sheet 15 of 20

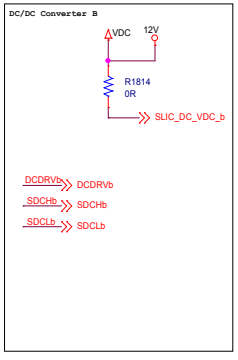


Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 16 of 20	

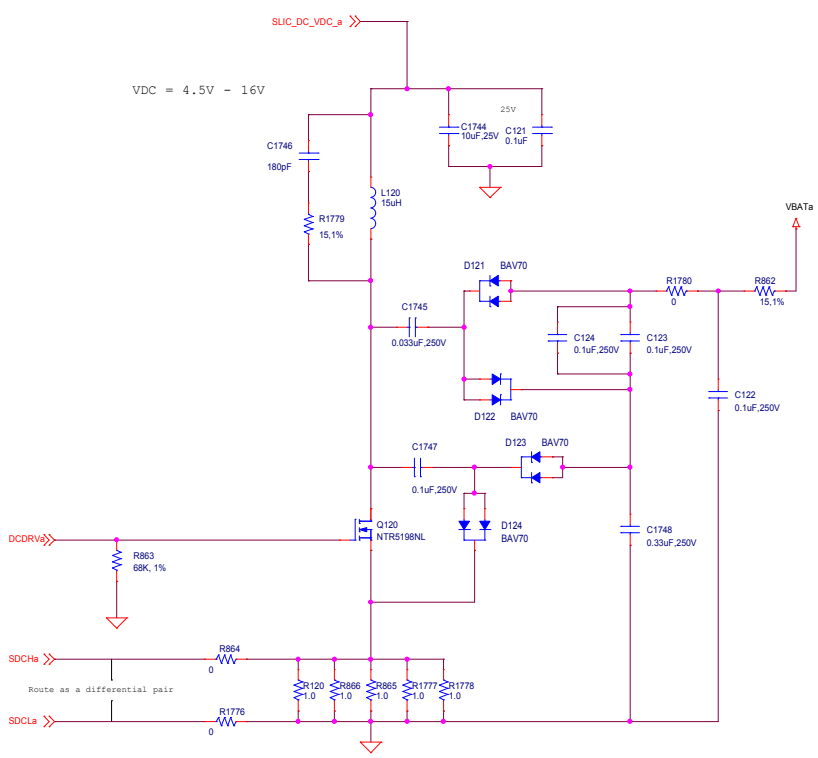


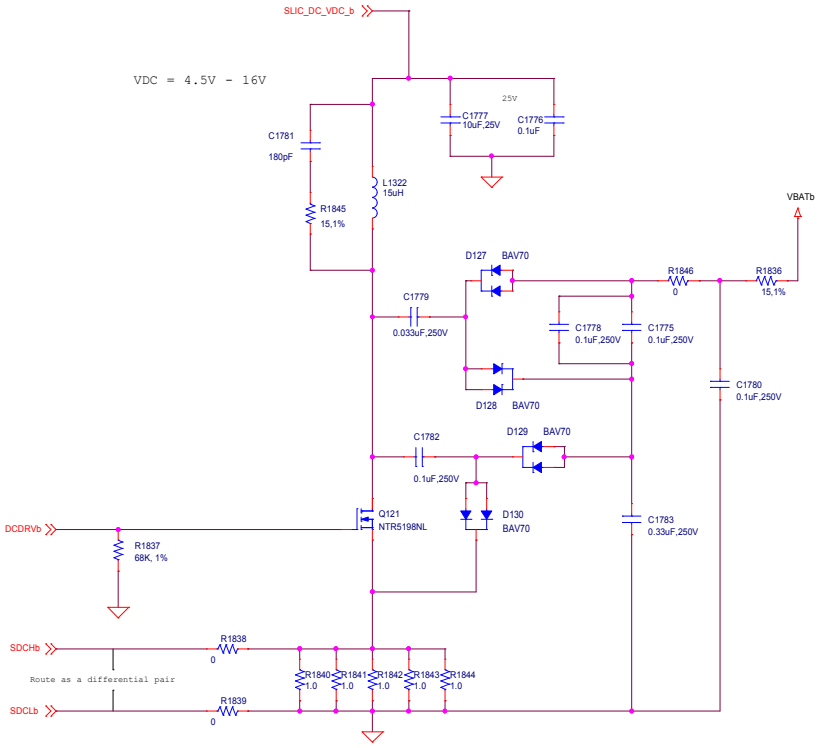


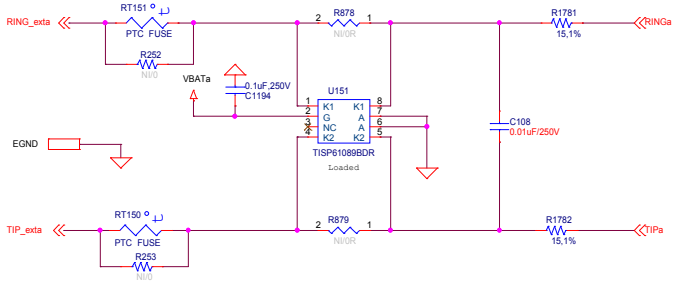


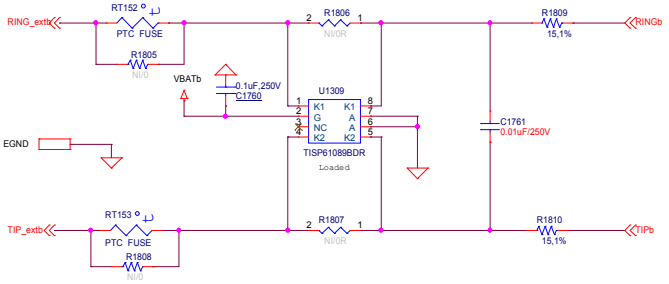


Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 17 of 20	





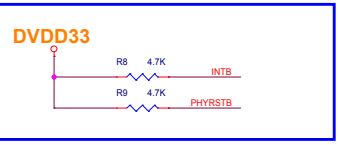




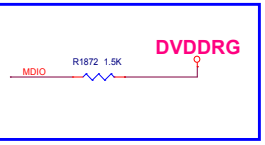
PTC will inherently have a resistance mismatch. This affects Longitudinal Balance. This means the PTC should be used in short loop applications where the longitudinal balance is not as important. In addition if the PTC ever fires its resistance will change quite a bit. This will affect the audio performance.

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 18 of 20	

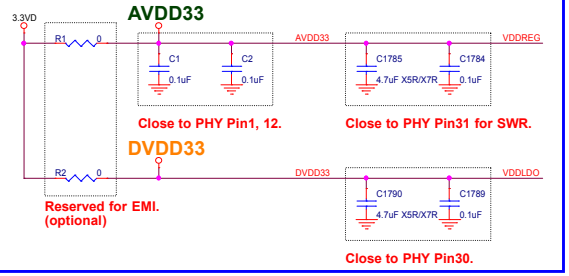
PHY RESET/INTB



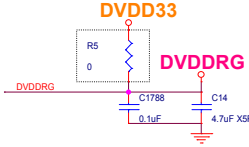
MDIO



3.3V Power Supply



RGMII Power



Note 1: R5 is not needed for ONLY 3.3V RGMII application, and DVDDRG can be connected directly to DVDD33.

Note 2: DVDDRG must be short (or R5 be mounted) to DVDD33 if the external RGMII 3.3V is selected.

Note 3: R5 must be removed if the internal 2.5V/1.8V/1.5V RGMII is selected.

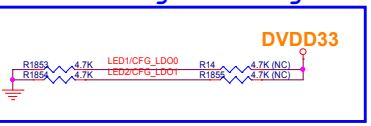
Note 4: CAPs must be closed to pin29 for EMI consideration.

RGMII RXC Delay Config.

Pull-up for additional 2ns delay to RXC for data latching.

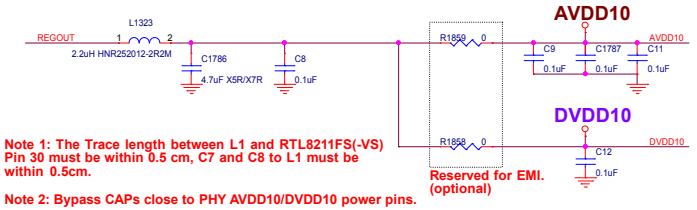
RSET

RGMII Voltage Config.



RGMII Power Source	CFG_LDO[1:0]
External 3.3V (default)	2'b00
Internal 2.5V	2'b01
Internal 1.8V	2'b10
Internal 1.5V	2'b11

Switching Regulator

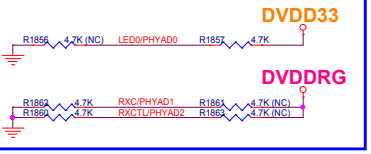


Note 1: The Trace length between L1 and RTL8211FS(-VS) Pin 30 must be within 0.5 cm, C7 and C8 to L1 must be within 0.5cm.

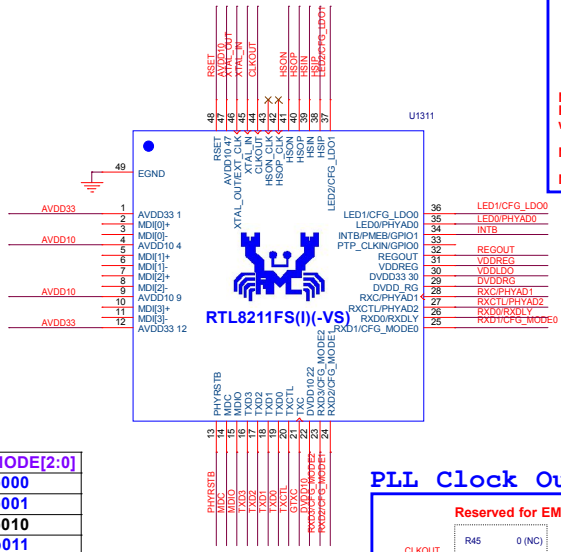
Note 2: Bypass CAPs close to PHY AVDD10/DVDD10 power pins.

Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.

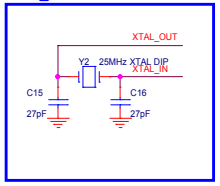
PHY Address Config.



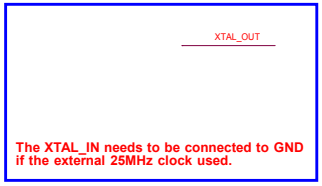
PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111



Crystal Case

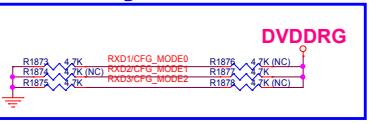


External clock Case



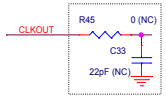
The XTAL_IN needs to be connected to GND if the external 25MHz clock used.

PHY Config.



Operating Mode	CFG_MODE[2:0]
UTP <=> RGMII	3'b000
FIBER <=> RGMII	3'b001
UTP/FIBER <=> RGMII	3'b010
UTP <=> SGMII	3'b011
SGMII (PHY) <=> RGMII	3'b100
SGMII (MAC) <=> RGMII	3'b101
UTP <=> FIBER (AUTO) (default)	3'b110
UTP <=> FIBER (FORCE)	3'b111

PLL Clock Out

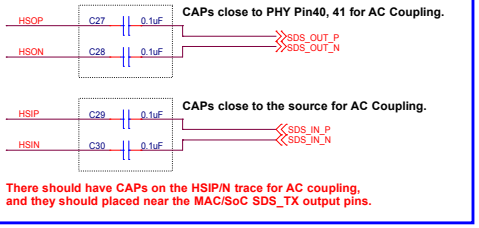


1. PLL Free run clock
2. UTP Recovered RXC for Sync Ethernet
3. Fiber Recovered RXC for Sync Ethernet
4. PTP clock output (RTL8211FS-VS Only)

SMA Connector is reserved for measurement. (optional)

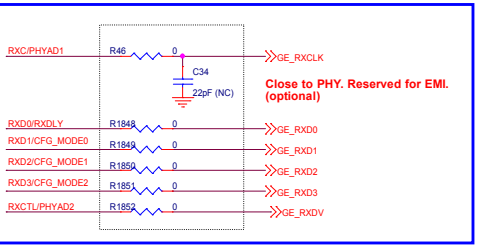
CAP close to PHY. Reserved for EMI. (optional)

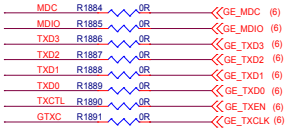
SERDES



There should have CAPs on the HSIP/N trace for AC coupling, and they should placed near the MAC/SoC SDS_TX output pins.

RGMII RX Filter Network

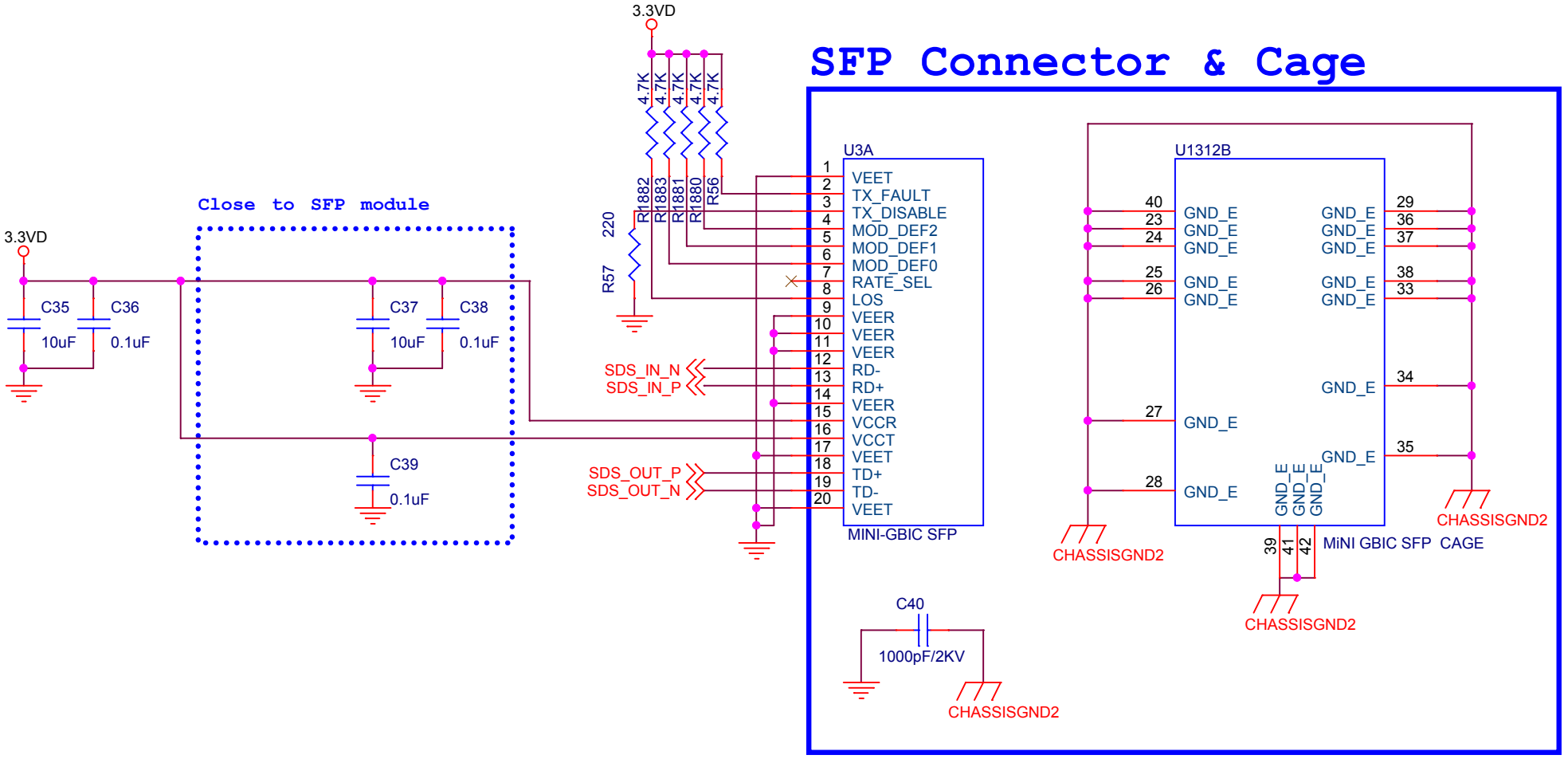




	LED Resistances Setting
PHYAD0=1'b1	R29(NC), R30, R31, R32(NC)
PHYAD0=1'b0	R29, R30(NC), R31(NC), R32
CFG_LDO0=1'b1	R33(NC), R34, R35, R36(NC)
CFG_LDO0=1'b0	R33, R34(NC), R35(NC), R36
CFG_LDO1=1'b1	R37(NC), R38, R39, R40(NC)
CFG_LDO1=1'b0	R37, R38(NC), R39(NC), R40

Title	<Title>	
Size C	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 19 of 20	

SFP Connector & Cage



Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Tuesday, September 22, 2020	Sheet 20 of 20	