MT7612
802.11 b/g/n/ac Wi-Fi single chip EEPROM Content

Version: 1.04
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Document Revision History

Revision	Date	Author	Description
0.0	2013/07/09	AlexCC Lin	Initial version
1.01	2013/10/11	SP Hsu	Update initial value and description for TC function
1.02	2013/11/21	SP Hsu	Update TC function example (0xF2~0xF5) Update eLNA gain description (0x44,0x45,0x49,0x4D) Update NIC setting description (0x25)
1.03	2014/01/06	SP Hsu	Modify 0x43 Xtal option description Add 0x9E for Xtal offset compensation feature Add 0x1C0/0x1C1 description Modify USB string description index (0x1D6~0x1DF) Modify 0x04 MAC address description Add 0x1B8~0x1BF Serial Number for Customer description
1.04	2014/06/13	William Lien	Update 0xB6~0xB9 description for configured 5G Channels.

Table of Contents

1 General Description

1.1 General Descriptions

The MT7612 EEPROM layout provides configuration for vendor/product ID, SW setting, RF TX power setting.

Note :
If hardware selects external EEPROM, please follow below EEPROM type.

The following table summarizes EEPROM used in MT7612 series configuration.

		EEPROM Type	EEPROM size (in byte)
MT7612E	2x2 ac, WIFI @PCIe	93c66	512
MT7612U	2x2 ac, USB3	25060	512

2 MT7612 EEPROM Layout

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	7662	Chip ID	
02h	0000	EEPROM Version	
04h	0000	Mac Address [15:8] Address 1	Mac Address [7:0] Address 0
06h	0000	Mac Address [31:24] Address 3	Mac Address [23:16] Address 2
08h	0000	Mac Address [47:40] Address 5	Mac Address [39:32] Address 4
0Ah	7612	WLAN PCIe Device ID	
0Ch	14C3	WLAN PCIe Vendor ID	
0Eh	0000	ASIC Reserved	
10h	0000	ASIC Reserved	
12h	7612	WLAN PCIe subsystem ID	
14h	14C3	WLAN PCIE subsystem VendorID	
16h	0000	ASIC Reserved	
18h	0000	ASIC Reserved	
1Ah	FFFF	ASIC Reserved	
1Ch	FFFF	ASIC Reserved	
1Eh	FFFF	ASIC Reserved	
20h	FFFF	ASIC Reserved*	
22h	D837	ASIC Reserved*	
24h	009D	For wifi external component setting	AUX Option
26h	7FFF	ASIC Reserved*	
28h	9BFD	ASIC Reserved*	
2Ah	FFFF	ASIC Reserved*	
2Ch	FFFF	ASIC Reserved*	
2Eh	FFFF	ASIC Reserved*	
30h	FFFF	ASIC Reserved*	
32h	FFFF	ASIC Reserved*	
34h	FF22	NIC Configuration 0	
36h	2000	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	Country Region 5G band
3Ah	0180	LED Mode	Frequency offset
3Ch	0000	LED Reserved	

Offset	Default (hex)	b15 ~b8	b7 ~ b0
3Eh	0000	LED Reserved	
40h	0000	LED Reserved	
42h	D7FF	NIC Configuration 2	
44h	0000	External LNA gain for 5G Band(CH36~CH64)	External LNA gain for 2.4G Band
46h	0000	2.4G RSSI1 offset	2.4G RSSI0 offset
48h	0000	External LNA gain for 5G Band(CH100~CH128)	Reserved
4Ah	0000	5G RSSI1 offset	5G RSSI0 offset
4Ch	000F	External LNA gain for 5GBand (CH132~CH165)	ASIC Reserved*
4Eh	0000	ASIC Reserved*	ASIC Reserved*
50h		20M/40M BW Power delta for 5G band	20M/40M BW Power delta for 2.4G band
52h		2G ePA temperature compensation limit	20M/80M BW Power delta for 5G band
54h		Thermal sensor value	5G ePA temperature compensation limit
56h		TX0 2.4G PA TSSI offset	TX0 2.4G PA TSSI slope
58h		TX0 2.4G TX power offset low	TX0 2.4G TX power (TSSI on) TX0 2.4G TX ALC CODE (TSSI off)
5Ah		TX0 2.4G TX power offset high	TX0 2.4G TX power offset middle
5Ch		TX1 2.4G PA TSSI offset	TX1 2.4G PA TSSI slope
5Eh		TX1 2.4G TX power offset low	TX1 2.4G TX power (TSSI on) TX1 2.4G TX ALC CODE (TSSI off)
60h		TX1 2.4G TX power offset high	TX1 2.4G TX power offset middle
62h		TX0 5G PA TSSI offset (Group0)	TX0 5G PA TSSI slope(Group0)
64h		TX0 5G TX power offset low(Group0)	TX0 5G TX power(Group0) (TSSI on) TX0 5G TX ALC CODE(Group0)(TSSI off)
66h		TX0 5G PA TSSI slope(Group1)	TX0 5G TX power offset high(Group0)
68h		TX0 5G TX power(Group1)(TSSI on) TX0 5G TX ALC CODE(Group1) (TSSI off)	TX0 5G PA TSSI offset (Group1)
6Ah		TX0 5G TX power offset high(Group1)	TX0 5G TX power offset low(Group1)
6Ch		TX0 5G PA TSSI offset (Group2)	TX0 5G PA TSSI slope(Group2)
6Eh		TX0 5G TX power offset low(Group2)	TX0 5G TX power(Group2) (TSSI on) TX0 5G TX ALC CODE(Group2)(TSSI off)
70h		TX0 5G PA TSSI slope(Group3)	TX0 5G TX power offset high(Group2)
72h		TX0 5G TX power(Group3) (TSSI on) TX0 5G TX ALC CODE(Group3)(TSSI off)	TX0 5G PA TSSI offset (Group3)
74h		TX0 5G TX power offset high(Group3)	TX0 5G TX power offset low(Group3)
76h		TX0 5G PA TSSI offset (Group4)	TX0 5G PA TSSI slope(Group4)
78h		TX0 5G TX power offset low(Group4)	TX0 5G TX power(Group4) (TSSI on) TX0 5G TX ALC code (Group4) (TSSI off)

Offset	Default (hex)	b15 ~b8	b7 ~ b0
7Ah		TX0 5G PA TSSI slope(Group5)	TX0 5G TX power offset high(Group4)
7Ch		TX0 5G TX power(Group5) (TSSI on) TX0 5G TX ALC code(Group5) (TSSI off)	TX0 5G PA TSSI offset (Group5)
7Eh		TX0 5G TX power offset high(Group5)	TX0 5G TX power offset low(Group5)
80h		TX1 5G PA TSSI offset (Group0)	TX1 5G PA TSSI slope(Group0)
82h		TX1 5G TX power offset low(Group0)	TX1 5G TX power(Group0) (TSSI on) TX1 5G TX ALC code (Group0) (TSSI off)
84h		TX1 5G PA TSSI slope(Group1)	TX1 5G TX power offset high(Group0)
86h		TX1 5G TX power(Group1) (TSSI on) TX1 5G TX ALC code(Group1) (TSSI off)	TX1 5G PA TSSI offset (Group1)
88h		TX1 5G TX power offset high(Group1)	TX1 5G TX power offset low(Group1)
8Ah		TX1 5G PA TSSI offset (Group2)	TX1 5G PA TSSI slope(Group2)
8Ch		TX1 5G TX power offset low(Group2)	TX1 5G TX power(Group2) (TSSI on) TX1 5G TX ALC CODE(Group2) (TSSI off)
8Eh		TX1 5G PA TSSI slope(Group3)	TX1 5G TX power offset high(Group2)
90h		TX1 5G TX power(Group3) (TSSI on) TX1 5G TX ALC CODE(Group3) (TSSI off)	TX1 5G PA TSSI offset (Group3)
92h		TX1 5G TX power offset high(Group3)	TX1 5G TX power offset low(Group3)
94h		TX1 5G PA TSSI offset (Group4)	TX1 5G PA TSSI slope(Group4)
96h		TX1 5G TX power offset low(Group4)	TX1 5G TX power(Group4) (TSSI on) TX1 5G TX ALC CODE(Group4) (TSSI off)
98h		TX1 5G PA TSSI slope(Group5)	TX1 5G TX power offset high(Group4)
9Ah		TX1 5G TX power(Group5) (TSSI on) TX1 5G TX ALC CODE(Group5) (TSSI off)	TX1 5G PA TSSI offset (Group5)
9Ch		TX1 5G TX power offset high(Group5)	TX1 5G TX power offset low(Group5)
9Eh		XTAL trim 2	XTAL Frequency offset compensation
A0h		2.4G TX power for CCK 5.5M/11M	2.4G TX power for CCK 1M/2M
A2h		2.4G TX power for OFDM 12M/18M	2.4G TX power for OFDM 6M/9M
A4h		2.4G TX power for OFDM 48M/54M	2.4G TX power for OFDM 24M/36M
A6h		2.4G/5G TX power for HT/VHT MCS=2,3	2.4G/5G TX power for HT/VHT MCS=0,1
A8h		2.4G/5G TX power for HT/VHT MCS=6,7	2.4G/5G TX power for HT/VHT MCS=4,5
AAh		2.4G/5G TX power for HT MCS10,11	2.4G/5G TX power for HT MCS8,9
ACh		2.4G/5G TX power for HT MCS14,15	2.4G/5G TX power for HT MCS12,13
AEh		Reserved	Reserved
B0h		Configured 2.4G Channels	Configured 2.4G Channels
B2h		5G Tx power for OFDM 12M/18M	5G Tx power for OFDM 6M/9M

Offset	Default (hex)	b15 ~b8	b7 ~ b0
B4h		5G Tx power for OFDM 48M/54M	5G Tx power for OFDM 24M/36M
B6h		Configured 5G Channels	Configured 5G Channels
B8h		Configured 5G Channels	Configured 5G Channels
BAh		Reserved	Reserved
BCh		Reserved	Reserved
BEh		TX power for 2.4G VHT MCS8,9	TX power for 5G VHT MCS8,9
F2h		5G ePA NT to low temp slope	5G ePA NT to high temp slope
F4h		2G ePA NT to low temp slope	2G ePA NT to high temp slope
F6h		TSSI off 2G TX power SKU (54M dBm)	Reserved
F8h		RF0/1 2.4G RX High Gain Internal use	TSSI off 5G TX power SKU (54M dBm)
FAh		RF0/1 5G RX High Gain (Group1) Internal use	RF0/1 5G RX High Gain (Group0) Internal use
FCh		RF0/1 5G RX High Gain (Group3) Internal use	RF0/1 5G RX High Gain (Group2) Internal use
FEh		RF0/1 5G RX High Gain (Group5) Internal use	RF0/1 5G RX High Gain (Group4) Internal use
130h		ASIC Reserved*	ASIC Reserved*
132h		ASIC Reserved*	ASIC Reserved*
134h		ASIC Reserved*	ASIC Reserved*
136h		ASIC Reserved*	ASIC Reserved*
138h			
13Ah			
13Ch			
1B8h		Serial number for customer	
1BAh		Serial number for customer	
1BCh		Serial number for customer	
1BEh		Serial number for customer	
1C0h	0300	USB BCD	USB BCD
1C2h	0E8D	USB descriptor : idVendor	
1C4h	7612	USB descriptor : idProduct	
1C6h	0100	ASIC reserved	ASIC Reserved
1C8h	00B4	ASIC reserved	ASIC reserved
1CAh	000A	ASIC reserved	ASIC reserved

Offset	Default (hex)	b15 ~b8	b7 ~ b0
1CCh	64A0	USB descriptor : Max Power	ASIC reserved
1CEh	0001	ASIC reserved	ASIC reserved
1D0h	FF3F	ASIC reserved	ASIC reserved
1D2h	1E08	ASIC reserved	ASIC reserved
1D4h	00F4	ASIC reserved	ASIC reserved
1D6h	FFFF	USB descriptor : String descriptor	USB descriptor : String descriptor
1D8h	FFFF	USB descriptor : String descriptor	USB descriptor : String descriptor
1DAh	FFFF	USB descriptor : String descriptor	USB descriptor : String descriptor
1DCh	FFFF	USB descriptor : String descriptor	USB descriptor : String descriptor
1DEh	FFFF	USB descriptor : String descriptor	USB descriptor : String descriptor

2.1 E2PROM layout version # (02h)

Value	Description
0	Version 0.
1 ~ 255	Invalid version. Treat as version 0.

2.2 WiFi External Component Setting (0x25)

Offset	Field	Description
25h	4:0	Reserved.
	7:5	000: No external RF component GPIO (iPAiLNA) 010 : Support external RF component GPIO (ePAeLNA) 110 : Internal PA 3 antenna mode for WIFI BT combo chip

External component GPIO usage will need to co-setting with 0x35 and 0x36.

2.3 NIC Configuration 0 (0x34/0x35)

0x35								0x34							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved		Board type		Reserved	PA driving	External PA		TX Path setting				RX Path setting			
Reserved		Reserved		Reserved	PA driving			1:1TX 2: 2TX				1: 1RX 2: 2RX			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
34h	3:0	RX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 RX front-end in the system. 2 (0010): 2 RX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 TX front-end in the system. 2 (0010): 2 TX front-end in the system. 3~ F (0011 ~ 1111): Reserved.

Offset	Field	Description
35h	1:0	external PA 00: 2.4G+5G external PA 01: 5G external PA 10: 2.4G external PA 11: disable
	2	External PA current setting – the IO driving current setting for external PA control pin 1: 8 mA (default) 0: 16mA
	3	Reserved.
	5:4	Reserved for define the board type.
	7:6	Reserved.

2.4 NIC Configuration 1 (0x36/0x37)

Bit[7:0]=0xFF will be treated as INVALID and used Default Value.
Bit[15:8]=0xFF will be treated as INVALID and used Default Value

0x36							
7	6	5	4	3	2	1	0
WPS PBC	5G side band for 40M BW	2.4G side band for 40M BW	Proprietary Test bit	EXT LNA 5G	EXT LNA 2.4G	Tx temp. scheme en	HW CTRL
0: off (D) 1: on	0: off(D) 1: on	0: off 1: on(D)	0: off(D) 1: on	0: off 1: on	0: off 1: on	0: off(D) 1: on	0: off(D) 1: on

0x37							
7	6	5	4	3	2	1	0
DAC test bit	BT Coexist	TSSI Power compensation en	Internal used		Broadband EXT LNA	40M BW in 5G band	40M BW in 2.4G band
0: off (D) 1: on	0: off (D) 1: on	0: off(D) 1: on	00: Disable (D)		0: off 1: on	0: on (D) 1: off	0: on (D) 1: off

NIC Configuration 1 Register Bit Fields Description

Offset	Field	Description

Offset	Field	Description
36h	0	Hardware Radio Control. 0: disable hardware radio control (default value). 1: enable hardware radio control. When “hardware radio control” bit is enabled (=1), the driver will read MAC’s GPIO status. When GPIO pin is low, the radio is disabled. When GPIO pin is high, the radio is enabled. The Radio ON/OFF is controlled by both software UI and MAC’s GPIO pin.
	1	TX power temperature compensation scheme enable (TC enable) 0 : disable temperature compensation 1 : Enable temperature compensation This bit will disable/enable temperature compensation scheme. While this bit is enable, it means Tx power TSSI scheme is disable(0x37 bit5 = 0) and using TC scheme. User must fill 0x53~0x54 and 0xF2~0xF5 for TC usage.
	2	External 2.4GHz band LNA. 0: Board without external LNA for 2.4GHz band must set this bit to 0. 1: Board with external LNA for 2.4GHz band must set this bit to 1 (default value).
	3	External 5GHz band LNA. 0: Board without external LNA for 5GHz band must set this bit to 0. 1: Board with external LNA for 5GHz band must set this bit to 1.
	4	Proprietary TEST BIT. For debug purpose. Default value is 0.
	5	2.4GHz side band for 40MHz BW. For debug purpose.
	6	5G side band for 40M BW For debug purpose.
	7	WPS Push Button Configuration control. 0: disable WPS PBC control (default value). 1: enable WPS PBC control. The WPS PBC function is controlled through GPIO[11]. If LED mode set to “Signal strength”(64), WPS PBC will be disabled.
37h	0	40M BW in 2.4GHz band. 0: enable 40MHz bandwidth for 2.4GHz band 1: disable 40MHz bandwidth for 2.4GHz band

Offset	Field	Description
	1	40M BW in 5G band 0: enable 40MHz bandwidth for 5GHz band. 1: disable 40MHz bandwidth for 5GHz band.
	2	Broadband EXT LNA 0: Board without external LNA must set this bit to 0. 1: Board with external LNA must set this bit to 1.
	4:3	Internal used Bit[12:11]: 00: default value
	5	TSSI power compensation enable 0 : disable TSSI power compensation , use per-group ALC code , like ePA case 1 : enable TSSI power compensation, TSSI slop offset scheme.
	6	BT Coexist 0: Disable BT coexistence. 1: Enable BT coexistence.
	7	DAC test bit 0: Disable DAC test. 1: Enable DAC test.

2.5 Country Region Code for 5G band(0x38)

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. therefore, FFh is our default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	36, 40, 44, 48, 52, 56, 60, 64, 149, 153, 157, 161, 165
1	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140
2	36, 40, 44, 48, 52, 56, 60, 64
3	52, 56, 60, 64, 149, 153, 157, 161

4	149, 153, 157, 161, 165
5	149, 153, 157, 161
6	36, 40, 44, 48
7	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165
8	52, 56, 60, 64
9	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 132, 136, 140, 149, 153, 157, 161, 165
10	36, 40, 44, 48,149, 153, 157, 161, 165
11	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 149, 153, 157, 161
12	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140
13	52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161
14	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 136, 140, 149, 153, 157, 161, 165
15	149, 153, 157, 161, 165, 169, 173
16	36, 40, 44, 48, 52, 56, 60, 64, 100, 104, 108, 112, 116, 120, 124, 128, 132, 136, 140, 149, 153, 157, 161, 165, 169, 173
30	Manual Channels (Refer to 0xB6h~B9h)

Note: 1.) If set to Index #12, it will also turn on 802.11h and Carrier Detection by default

2.) The index value is decimal system.

2.6 Country Region Code for 2.4G band (0x39)

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value. CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	CH 1 ~ 11
1	CH 1 ~ 13
2	CH 10 ~ 11
3	CH 10 ~ 13
4	CH 14
5	CH 1 ~ 14
6	CH 3 ~ 9

7	CH 5 ~ 13
30	Manual Channel (Refer to 0xB0h~B1h)
31	CH1 ~ 14 (CH1 ~ 11 active scan, CH12 ~ 14 passive scan)
32	CH1 ~ 13 (CH1 ~ 11 active scan, CH12 ~ 13 passive scan)
33	802.11b: CH1 to CH14 are active scan. 802.11g/n: CH1 to CH13 are active scan. CH14 is disallowed

Notes: If set to read SKU from EEPROM, only available if 2.4G Country Region code registers are programmed.

2.7 Frequency offset (0x3A)

Used for crystal calibration. 0x3A is used for MTK FT test only for crystal calibration-free feature.
MTK wafer manufactory used 0x3A, bit 0~6, to store frequency offset value which is measured under MTK FT environment. Each IC has each corresponding frequency offset .
If customers want to re-burn crystal trim value, please use 0x9F as 2nd crystal trim offset.

Offset	Field	Description
3Ah	6:0	Crystal trim value (Cap ID) K-free IC will fill value in MTK FT production line for each chip.
	7	0: DIP type 1: SMT type

2.8 LED Mode Setting (0x3B)

2.9 NIC Configuration 2 (0x42/0x43)

0x43					0x42							
Bit <7:5>	4	3	2:1	0	7	6	5	4	3	2	1	0
Co-exist stream mode	Reserved	25C Temperature Disable	Xtal option	HW Ant Div	TX Stream 1: 1 Stream 2: 2 Stream				RX Stream 1: 1 Stream 2: 2 Stream			

Note:
1. The 1 stream support MCS0~MCS7. The 2 stream support MCS0~MCS15.
2. Stream setting should be equal or less than path setting of EEPROM (0x34)
3. Default=0xFF means that based on the path setting (0x34) for MAX capability.

NIC Configuration 2 Register Bit Fields Description

Offset	Field	Description
42h	3:0	RX stream. 0 (0000): Reserved 1 (0001): 1 RX stream 2 (0010): 2 RX stream 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX stream. 0 (0000): Reserved 1 (0001): 1 TX stream 2 (0010): 2 TX stream 3 ~ F (0011 ~ 1111): Reserved.
43h	0	Not support
	2:1	Xtal option: 00 : reserved 01 : One crystal, enable co-clock out 10 : reserved 11 : default value
	3	25C Temperature disable bit 0 : Enable 1 : Disable
	4	Reserved.
	7:5	Reserved Co-exist stream mode : default is 110 1 : 1x1 , no co-exist , Pure BT 2 : 1T2R, no co-exist , Pure WIFI 3 : 1T2R, no co-exist, Pure WIFI 4 : WLAN 1x1 and BT co-exist , 5 : WLAN 2x2, no co-exist 6 : WLAN 2x2 and BT co-exist

2.10 External LNA Gain for 2.4GHz (0x44)

0x44							
7	6	5	4	3	2	1	0
Sign bit	External LNA Gain for 2.4G						

External LNA Gain for 2.4GHz Register Bit Fields Description

Offset	Field	Description
44h	6:0	External LNA gain for 2.4GHz 000000 : 0dB 000001 : 1dB 000010 : 2dB This value should be reasonable for external component spec. 111111 won't be invalid.
	7	Sign bit 1: plus " + " 0: minus " – "

Example:

The default eLNA gain value would be 0x8C and it means " +12dB".

2.11 External LNA Gain for 5GHz (0x45/0x49/0x4D)

0x45							
7	6	5	4	3	2	1	0
Sign bit	External LNA Gain for 5G(CH36~CH64)						
0x49							
7	6	5	4	3	2	1	0
Sign bit	External LNA Gain for 5G(CH100~CH128)						
0x4D							
7	6	5	4	3	2	1	0
Sign bit	External LNA Gain for 5G(CH132~CH165)						

External LNA Gain for 5GHz Register Bit Fields Description

Offset	Field	Description

Offset	Field	Description
45h 49h 4Dh	6:0	External LNA gain for 5GHz 000000 : 0dB 000001 : 1dB 000010 : 2dB This value should be reasonable for external component spec. 111111 won't be invalid.
	7	Sign bit 1: plus " + " 0: minus " – "

Example:

The default eLNA gain value would be 0x8C and it means " +12dB".

2.12 20M/40M BW Power Delta for 2.4GHz band (0x50h)

Driver compensates the TX power value of 40M BW with this configured value. (unit : 0.5dm)

TX power delta configuration Register Bit Fields Description

Offset	Field	Description
50h	5:0	40M BW TX power delta value (MAX=4dBm). 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101: 2.5dBm 000110: 3dBm 000111: 3.5dBm 001000: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
	7	1: enableTX power compensation.

Example:

The default calibrated TX power as followings with the TX power delta configuration is not enable.

- 40M BW TX power= 14dBm and 20M BW TX power = 14dBm

If want keep 20M BW TX power in 14dBm and reduce 40M BW TX power to 10dBm (delta=4dBm), set 50h = 88h (1000 1000).

2.13 20M/40M BW Power Delta for 5G band (0x51h)

Offset	Field	Description
0x51h	5:0	40M BW TX power delta value (MAX=4dBm). 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101: 2.5dBm 000110: 3dBm 000111: 3.5dBm 001000: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
	7	1: enable TX power compensation.

2.14 20M/80M BW Power Delta for 5G band (0x52h)

Offset	Field	Description
0x52h	5:0	80M BW TX power delta value (MAX=4dBm). 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101: 2.5dBm 000110: 3dBm 000111: 3.5dBm 001000: 4dBm
	6	1: increase 80M BW TX power with the delta value. 0: decrease 80M BW TX power with the delta value.
	7	1: enable TX power compensation.

2.15 Thermal Sensor Calibration (0x55h)

For K-free IC, thermal sensor calibration value will be filled in MTK FT production line.

Offset	Field	Description
0x55h	6:0	MTK FT Thermal sensor value
	7	1: Use temperature sensor calibration value 0: Not use temperature sensor calibration value

2.16 TX0 2.4G PA TSSI Slop /offset (0x56h~0x57h)

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value.
This function is controlled by 'TSSI power compensation enable' bit (0x37 bit5).
For K-free IC, TSSI offset and slope value will be filled in MTK FT production line.

2.17 TX0 2.4G Target Power/ALC code (0x58h)

It defines TX0 2.4G target power at 54M for TSSI on case. 1step = 0.5dB.
It defines TX0 2.4G ALC code 54M for TSSI off case.
Example:
TSSI on case
If system 54M target power is 13dBm setting, 13dBm= 13*2 = 26(dec) = 0x1A (hex).
0x58 offset should be filled with 0x1A.

TSSI off case
If DAC ALC code value 0x0D has 13dBm 54M power performance, 0x58 offset should be filled with 0x0D.
You might fill 0x1A value to 0xF7 offset for 2G SKU usage.

2.18 TX0 2.4G TX Power offset low/middle/high (0x59h~0x5Bh)

1step =0.5dB
Users could use TX power low/middle/high offset for power adjustment.
0x59 = CH1~CH5 range (low channels)
0x5A = CH6~CH10 range (middle channels)
0x5B = CH11~CH14 range (high channels)
Example:
If users want CH1 1dB higher than CH11, 0x59=0xC2 and 0x5B=0x00

Offset	Field	Description
59h ~5Bh	5:0	TX power offset (delta, dB)
	7:6	Bit[7] : enable

		Bit[6] : 0 : decrease power , 1 :increase power

2.19 Tx1 2.4G PA TSSI Power Slop /offset (0x5Ch~0x5Dh)

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value.
This function is controlled by 'TSSI power compensation enable' bit (0x37 bit5).For K-free IC, TSSI offset and slope value will be filled in MTK FT production line.

2.20 TX1 2.4G Target Power/ALC code (0x5Eh)

It defines TX1 2.4G target power at 54M for TSSI on case. 1step = 0.5dB.
It defines TX1 2.4G ALC code 54M for TSSI off case.
Example:
TSSI on case
If system 54M target power is 13dBm, 13dBm= 13*2 = 26(dec) = 0x1A(hex)
0x5E offset should be filled with 0x1A value.

TSSI off case
If DAC ALC code value 0x0D could get 13dBm 54M power,
0x5E offset should be filled with 0x0D value.
You might fill 0x1A value to 0xF7 offset for 2G SKU usage.

2.21 TX1 2.4G TX Power offset low/middle/high (0x5Fh~0x61h)

1step =0.5dB
Users could use TX power low/middle/high offset to do power adjustment.
0x5F = CH1~CH5 range(low channels)
0x60 = CH6~CH10 range (middle channels)
0x61 = CH11~CH14 range (high channels)
Example:
If users want to make CH1 1dB higher than CH11, 0x5F=0xC2 and 0x61=0x00

Offset	Field	Description
5Fh ~61h	5:0	TX power offset (delta, dB)
	7:6	Bit[7] : enable Bit[6] : 0 : decrease power , 1 :increase power

2.22 TX0 5G Goup0 PA TSSI Power Slop /offset (0x62h~0x63h)

Group0 = 4.9~5GHz range

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value.
This function is controlled by 'TSSI power compensation enable' bit (0x37 bit5).For K-free IC, TSSI offset and slope value will be filled in MTK FT production line.

2.23 TX0 5G Group0 Target Power/ALC code (0x64h)

It defines TX0 4.9~5G target power at 54M for TSSI on case. 1step = 0.5dB.
It defines the TX0 4.9~5G ALC code 54M for TSSI off case.
Example:
TSSI on case
If system 54M target power is 13dBm, 13dBm= 13*2 = 26(dec) = 0x1A(hex)
0x64 offset should be filled with 0x1A value.

TSSI off case
If DAC ALC code value 0x0D could get 13dBm 54M power,
0x64 offset should be filled with 0x0D value.
But you might fill 0x1A to 0xF8 offset for 5G SKU usage.

2.24 TX0 5G Group0 TX Power offset low/high (0x65h~0x66h)

1step =0.5dB
Users could use TX power low/middle/high offset to do power adjustment.
0x65 = CH184~CH188 range(low channels)
0x66 = CH192~CH196 range (high channels)
Example:
If users want to make CH184 1dB higher than CH196, 0x65=0xC2 and 0x66=0x00

Offset	Field	Description
65h ~66h	5:0	TX power offset (delta, dB)
	7:6	Bit[7] : enable Bit[6] : 0 : decrease power , 1 :increase power

2.25 TX0 5G Goup1 PA TSSI Power Slop /offset (0x67h~0x68h)

Group1 = 5.18~5.24GHz range

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value.

This function is controlled by 'TSSI power compensation enable' bit (0x37 bit5).For K-free IC, TSSI offset and slope value will be filled in MTK FT production line.

2.26 TX0 5G Group1 Target Power/ALC code (0x69h)

It defines TX0 5.18~5.24G target power at 54M for TSSI on case. 1step = 0.5dB.
It defines the TX0 5.18~5.24G ALC code 54M for TSSI off case.
Example:
TSSI on case
If system 54M target power is 13dBm, 13dBm= 13*2 = 26(dec) = 0x1A(hex)
0x69 offset should be filled with 0x1A value.

TSSI off case
If DAC ALC code value 0x0D could get 13dBm 54M power,
0x69 offset should be filled with 0x0D value.
But you might fill 0x1A to 0xF8 offset for 5G SKU usage.

2.27 TX0 5G Group1 TX Power offset low/high (0x6Ah~0x6Bh)

1step =0.5dB
Users could use TX power low/middle/high offset to do power adjustment.
0x6A = CH36~CH42 range (low channels)
0x6B = CH44~CH48 range (high channels)
Example:
If users want to make CH36 1dB higher than CH48, 0x6A=0xC2 and 0x6B=0x00

Offset	Field	Description
6Ah ~6Bh	5:0	TX power offset (delta, dB)
	7:6	Bit[7] : enable Bit[6] : 0 : decrease power , 1 :increase power

2.28 5G Group0~5 Offset Channel Mapping (0x62~0x9D)

For detail field description, please see 2.12~2.23

Offset	Description
0x62	TX0 5G PA TSSI slope (4920~4980)(CH184 188 192 196)
0x63	TX0 5G PA TSSI offset (4920~4980)(Group0)
0x64	TX0 5G TX power Group0 (54M TSSI on) (4920~4980) TX0 5G TX ALC code Group0(54M TSSI off) (4920~4980)
0x65	TX0 5G TX power offset low(delta,dB)(CH184 188)
0x66	TX0 5G TX power offset high(delta,dB)(CH 192 196)
0x67	TX0 5G PA TSSI slope (5150~5250) (CH36 38 40 42 44 46 48)
0x68	TX0 5G PA TSSI offset (5150~5250)(Group1)
0x69	TX0 5G TX power Group1 (54M TSSI on)(5150~5250) TX0 5G TX ALC code Group1 (54M TSSI off)(5150~5250)
0x6A	TX0 5G TX power offset low(delta,dB) (CH36 38 40 42)
0x6B	TX0 5G TX power offset high(delta,dB) (CH44 46 48)
0x6C	TX0 5G PA TSSI slope (5250~5350) (CH52 54 56 58 60 62 64)
0x6D	TX0 5G PA TSSI offset (5250~5350)(Group2)
0x6E	TX0 5G TX power Group2 (54M TSSI on) (5250~5350) TX0 5G TX ALC code Group2(54M TSSI off) (5250~5350)
0x6F	TX0 5G TX power offset low(delta,dB)(CH52 54 56)
0x70	TX0 5G TX power offset high(delta,dB)(CH58 60 62 64)

0x71	TX0 5G PA TSSI slope (5480~5570)(CH100 101 104 106 108 112 114)
0x72	TX0 5G PA TSSI offset (5480~5570)(Group3)
0x73	TX0 5G TX power Group3 (54M TSSI on)(5480~5570) TX0 5G TX ALC code Group3 (54M TSSI off)(5480~5570)
0x74	TX0 5G TX power offset low(delta,dB)(CH100 101 104)
0x75	TX0 5G TX power offset high(delta,dB)(CH106 108 112 114)
0x76	TX0 5G PA TSSI slope (5580~5700)(CH116 120 122 124 128 130 132 136 138 140 144)
0x77	TX0 5G PA TSSI offset (5580~5700)(Group4)
0x78	TX0 5G TX power Group4 (54M TSSI on) (5580~5700) TX0 5G TX ALC code Group4(54M TSSI off) (5580~5700)
0x79	TX0 5G TX power offset low(delta,dB)(CH116 120 122 124 128)
0x7A	TX0 5G TX power offset high(delta,dB)(CH130 132 136 138 140 144)
0x7B	TX0 5G PA TSSI slope (5725~5825)(CH149 153 155 156 157 161 162 165)
0x7C	TX0 5G PA TSSI offset (5725~5825)(Group5)
0x7D	TX0 5G TX power Group5 (54M TSSI on)(5725~5825) TX0 5G TX ALC code Group5 (54M TSSI off)(5725~5825)
0x7E	TX0 5G TX power offset low(delta,dB) (CH149 153 155 156)
0x7F	TX0 5G TX power offset high(delta,dB)(CH157 161 162 165)
0x80	TX1 5G PA TSSI slope (4920~4980)(CH184 188 192 196)
0x81	TX1 5G PA TSSI offset (4920~4980)(Group0)
0x82	TX1 5G TX power Group0 (54M TSSI on) (4920~4980) TX1 5G TX ALC code Group0(54M TSSI off) (4920~4980)
0x83	TX1 5G TX power offset low(delta,dB)(CH184 188)
0x84	TX1 5G TX power offset high(delta,dB)(CH 192 196)
0x85	TX1 5G PA TSSI slope (5150~5250) (CH36 38 40 42 44 46 48)
0x86	TX1 5G PA TSSI offset (5150~5250)(Group1)
0x87	TX1 5G TX power Group1 (54M TSSI on)(5150~5250) TX1 5G TX ALC code Group1 (54M TSSI off)(5150~5250)
0x88	TX1 5G TX power offset low(delta,dB) (CH36 38 40 42)
0x89	TX1 5G TX power offset high(delta,dB) (CH44 46 48)
0x8A	TX1 5G PA TSSI slope (5250~5350) (CH52 54 56 58 60 62 64)
0x8B	TX1 5G PA TSSI offset (5250~5350)(Group2)
0x8C	TX1 5G TX power Group2 (54M TSSI on) (5250~5350) TX1 5G TX ALC code Group2(54M TSSI off) (5250~5350)
0x8D	TX1 5G TX power offset low(delta,dB)(CH52 54 56)
0x8E	TX1 5G TX power offset high(delta,dB)(CH58 60 62 64)
0x8F	TX1 5G PA TSSI slope (5480~5570)(CH100 101 104 106 108 112 114)
0x90	TX1 5G PA TSSI offset (5480~5570)(Group3)

0x91	TX1 5G TX power Group3 (54M TSSI on)(5480~5570) TX1 5G TX ALC code Group3 (54M TSSI off)(5480~5570)
0x92	TX1 5G TX power offset low(delta,dB)(CH100 101 104)
0x93	TX1 5G TX power offset high(delta,dB)(CH106 108 112 114)
0x94	TX1 5G PA TSSI slope (5580~5700)(CH116 120 122 124 128 130 132 136 138 140 144)
0x95	TX1 5G PA TSSI offset (5580~5700)(Group4)
0x96	TX1 5G TX power Group4 (54M TSSI on) (5580~5700) TX1 5G TX ALC code Group4(54M TSSI off) (5580~5700)
0x97	TX1 5G TX power offset low(delta,dB)(CH116 120 122 124 128)
0x98	TX1 5G TX power offset high(delta,dB)(CH130 132 136 138 140 144)
0x99	TX1 5G PA TSSI slope (5725~5825)(CH149 153 155 156 157 161 162 165)
0x9A	TX1 5G PA TSSI offset (5725~5825)(Group5)
0x9B	TX1 5G TX power Group5 (54M TSSI on)(5725~5825) TX1 5G TX ALC code Group5 (54M TSSI off)(5725~5825)
0x9C	TX1 5G TX power offset low(delta,dB) (CH149 153 155 156)
0x9D	TX1 5G TX power offset high(delta,dB)(CH157 161 162 165)

2.29 XTAL Frequency Offset Compensation (0x9Eh)

If Xtal layout is not close to IC but customers still want to take K-free result as reference to reduce test time, customers need to find out the offset value between new target XTAL capID and origin K-free capID.

For example

Origin K-free capID on 0x3A offset is 0x42 and measured frequency is -10ppm on customer‘s new PCB. Customers need to adjust capID from 0x42 to 0x62 to get 0ppm result and we could get the offset is 0x20. If customers fill 0x20 to 0x9E E2P position, the final capID value is 0x42+0x20 in driver.

Offset	Field	Description
9Eh	6:0	Offset compensation
	7	Signed bit. For positive, it’s equal to 0 For negative, it’s equal to 1

2.30 XTAL trim 2 (0x9Fh)

It is the second xtal trim field provided for customer MP site.

1st one is 0x3A.

Offset	Field	Description

Offset	Field	Description
9Fh	6:0	Crystal trim value (Cap ID)
	7	Reserved

2.31 TX rate power configuration (0xA0h~0xBFh)

Default value=0x00 (1 step=0.5dBm)

Offset	Field	Description
A0h ~BFh	5:0	Tx per-rate power setting
	7:6	Bit[7] : enable Bit[6] : 0 : decrease power , 1 :increase power

Offset	Default Value	Description	Bit [5:0]
A0h	00	2G TX power for CCK 1M/2M	TX power setting
A1h	00	2G TX power for CCK 5.5M/11M	TX power setting
A2h	00	2G TX power for OFDM 6M/9M	TX power setting
A3h	00	2G TX power for OFDM 12M/18M	TX power setting
A4h	00	2G TX power for OFDM 24M/36M	TX power setting
A5h	00	2G TX power for OFDM 48M/54M	TX power setting
A6h	00	2/5G TX power for HT/VHT MCS=0,1	TX power setting
A7h	00	2/5G TX power for HT/VHT MCS=2,3	TX power setting
A8h	00	2/5G TX power for HT/VHT MCS=4,5	TX power setting
A9h	00	2/5G TX power for HT/VHT MCS=6,7	TX power setting
AAh	00	2/5G TX power for HT MCS=8,9	TX power setting
ABh	00	2/5G TX power for HT MCS=10,11	TX power setting
ACh	00	2/5G TX power for HT MCS=12,13	TX power setting
ADh	00	2/5G TX power for HT MCS=14,15	TX power setting
B2h	00	5G TX power for OFDM 6M/9M	TX power setting
B3h	00	5G TX power for OFDM 12M/18M	TX power setting
B4h	00	5G TX power for OFDM 24M/36M	TX power setting
B5h	00	5G TX power for OFDM 48M/54M	TX power setting
BEh	00	5G TX power for VHT M8/M9	TX power setting
BFh	00	2G TX power for VHT M8/M9	TX power setting

Example:

If the calibrated TX power =15dBm for 54Mbps = 0x00 (offset = A5h).

Want to set both TX power to 19dBm for MCS 0 & MCS 1 (offset = A6h).
The power difference is 4dBm (19-15). It need to increase register value from 0 to 8 (4dBm = 0.5dBm * 8 step). Setting A6h=0xC8h can meet the power requirement.

Offset	Suggest Value	Description
0xA0	C3	2.4GHz TX power for CCK 1M/2M(delta,dB)
0xA1	C3	2.4GHz TX power for CCK 5.5M/11M(delta,dB)
0xA2	C4	2.4GHz TX power for OFDM 6M/9M(delta,dB)
0xA3	C4	2.4GHz TX power for OFDM 12M/18M(delta,dB)
0xA4	0	2.4GHz TX power for OFDM 24M/36M(delta,dB)
0xA5	0	2.4GHz TX power for OFDM 48M/54M(delta,dB)
0xA6	C2	2.4/5G TX power for HT MCS=0,1(delta,dB)
0xA7	C2	2.4/5G TX power for HT MCS=2,3(delta,dB)
0xA8	82	2.4/5G TX power for HT MCS=4,5(delta,dB)
0xA9	82	2.4/5G TX power for HT MCS=6,7(delta,dB)
0xAA	C2	2.4/5G TX power for HT MCS8,9(delta,dB)
0xAB	C2	2.4/5G TX power for HT MCS10,11(delta,dB)
0xAC	82	2.4/5G TX power for HT MCS12,13(delta,dB)
0xAD	82	2.4/5G TX power for HT MCS14,15(delta,dB)
0xB2	C2	5GHz TX power for OFDM 6M/9M(delta,dB)
0xB3	C2	5GHz TX power for OFDM 12M/18M(delta,dB)
0xB4	0	5GHz TX power for OFDM 24M/36M(delta,dB)
0xB5	0	5GHz TX power for OFDM 48M/54M(delta,dB)
0xBE	83	TX power for 5GHz VHT MCS=8,9
0xBF	83	TX power for 2.4GHz VHT MCS=8,9

2.32 Configured 2.4G Channels (0xB0h~0xB1h)

Default value=0x00, this field is available when 0x39h = 30d. (Configured channel)

7	6	5	4	3	2	1	0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

15	14	13	12	11	10	9	8
Reserve	Reserve	CH14	CH13	CH12	CH11	CH10	CH9
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

For example:
If available channels are 1,2,3 and 5, then
0x39h = 30d, 0xB0h = 17h, 0xB1h = 00h.

2.33 Configured 5G Channels (0xB6h~0xB9h)

Default value=0x00, this field is available when 0x38h = 30d (Manual channel)

B6h

7	6	5	4	3	2	1	0
CH64	CH60	CH56	CH52	CH48	CH44	CH40	CH36
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

B7h

7	6	5	4	3	2	1	0
CH128	CH124	CH120	CH116	CH112	CH108	CH104	CH100
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

B8h

7	6	5	4	3	2	1	0
CH165	CH161	CH157	CH153	CH149	CH140	CH136	CH132
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

B9h

7	6	5	4	3	2	1	0
Reserve	Reserve	Reserve	Reserve	CH173	CH171	CH169	CH167
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

For example:
If available channels are 40, 48, 64, 116,161, 165 and 173, then
0x38h = 30d, 0xB6h = 8Ah, 0xB7h = 10h, 0xB8h = C0h, 0xB9h = 08h

2.34 Serial Number for Customer (0x1B8h~0x1BFh)

2.35 USB BCD (0x1C0~0x1C1h)

Offset	Field	Description
1C0h	7:0	0x00 for MT7612U
1C1h	7:0	0x03 for MT7612U

2.36 USB Vendor ID (0x1C2~0x1C3h)

Value	Description
0x0E8D	The default Vendor ID for MTK

If customers need to change USB PID/VID, need to fill proper value for 0x1C0 ~0x1DF offset.

2.37 USB Product ID (0x1C4h~0x1C5h)

Value	Description
0x7612	The default Product ID for MTK

If customers need to change USB PID/VID, need to fill proper value for 0x1C0 ~0x1DF offset.

2.38 USB String Descriptor Index (0x1D6h~0x1DFh)

Offset	Field	Description
1D6h	7:0	USB descriptor string index (high byte part): It's the string start address high byte part. For example, the string index start address is 0x140. 0x01 is the string index head, the low byte will indicate on 0x1D7h~0x1DFh . 0x1D7 is offset of string index 1, 0x1D8 is offset of string index 2, and so on.
1D7h~1DEh	7:0	The USB descriptor string index (low byte part): it concatenate with 0x1D6h to indicate the string address in EEPROM. It provides 9 string index fields. Customer can update USB string on EEPROM's empty field (0x140~0x1BF is preferred field) and modify the string start address on these string descriptor index. The string indexes should be continuous. For example : At EEPROM 0x140 has one String ("802.11n WLAN") for string index 2 , it should be: 1E 03 38 00 30 00 32 00 2E 00 31 00 31 00 20 00 6E 00 20 00 57 00 4C 00 41 00 4E 00 "1E" is the string length, "03" is the String type, then each two bytes indicate the uni-code of each character. And please update 0x1D6h = 0x01, 0x1D8h = 0x40 to indicate the string index 2.

2.39 2G/5G Temperature Compensation Enable/Disable (0x36,0x43,0x55)

There are 3 EEPROM setting needs to be configured for temperature compensation. Main purpose is for ePAiPA RFCR switch, BB CR switch, RF re-cal of IC performance variation over temperature.

1. 0x36 bit1 :
   i. 1: enable TC for TX PA power setting
   ii. 0 : disable TC for TX PA power setting
2. 0x43 bit3 :
   i. 0 :enable TC for BB/RF CR switch
   ii. 1 : disable TC for BB/RF CR switch setting
3. 0x55 bit7
   i. 1: enable temperature sensor value
   ii. 0 : disable temperature sensor value
4. 0x55 bit[6:0]
   i. Thermal sensor value: This value will be filled in MTK FT production line. Customers don't need to re-fill this column.

2.40 2G/5G ePA Temperature Compensation limit(0x53h~0x54h)

Temperature compensation will be constraint within Temperature compensation configures in 0x53h~0x54h. Resolution is 1dB/step.

1. Use 0x53[7:4] for 2G temperature compensation upper limit for high temperature gain variation
2. Use 0x53[3:0] for 2G temperature compensation lower limit for low temperature gain variation.
3. Use 0x54[7:4] for 5G temperature compensation upper limit for high temperature gain variation.
4. Use 0x54[3:0] for 5G temperature compensation lower limit for low temperature gain variation
5. Fill up 2/5G high/low limit with positive value, because lower limit is negative value in actual, software will transfer lower limit to negative value in driver
   For example:
   If user would like to set upper limit to 4dB and lower limit -7dB in 5G band, fill up 0x54[7:4]=0x04 and 0x54[3:0]=0x07.
   Please apply the same method in 2G according to 2G design.
6. If limit value is equal to 0x00 or 0xFF, temperature compensation will be disable
7. Unit of Temperature compensation limit: (dB)
   If you use MTK HDK, you could use value as follows.

Offset	Field	Description
0x53	3:0	2G TC gain low limit for NT to LT
	7:4	2G TC gain high limit for NT to HT
0x54	3:0	5G TC gain low limit for NT to LT
	7:4	5G TC gain high limit for NT to HT

Offset	Value	Description
0x53	0x57	2G ePA Temperature Compensation limit
0x54	0x47	5G ePA Temperature Compensation limit

2.41 2G/5G ePA Slope for Temperature Compensation (0xF2h~0xF5h)

Offset	Description

0xF2	5G ePA NT to high temp slope
0xF3	5G ePA NT to low temp slope
0xF4	2G ePA NT to high temp slope
0xF5	2G ePA NT to low temp slope

1. Fill up 2/5G ePA NT to high temp slope and NT to low temp slope value with positive value slope
2. If Slope value equals to 0x00 or 0xFF, temperature compensation will be disable
3. Unit of Slope: (℃/dB)

Example:
If gain difference between NT and HT is 4dB, the slope of +25 degree C to 85 degree C is equal to 15
(85-25)/4=15(dec)=0x0F(hex)
If gain difference between NT and LT is 5dB, the slope of +25 degree C to -20 degree C is equal to 9
((25-(-20))/5=9(dec)=0x09(hex)

If you use MTK HDK, you could use value as follows.

Offset	Value	Description
0xF2	0F	5G ePA NT to high temp slope
0xF3	09	5G ePA NT to low temp slope
0xF4	0D	2G ePA NT to high temp slope
0xF5	10	2G ePA NT to low temp slope

2.42 TSSI off 2.4/5G TX power SKU (0xF7, 0xF8)

Unit: 0.5dBm
Driver will use this value as reference target power of SKU function.

TSSI off:
If 5G 54M target power is 13dBm, 13dBm= 13*2 = 26(dec) = 0x1A(hex)
0xF8 offset should be filled with 0x1A value.

Offset	Description
0xF7	TSSI off 2.4G TX power (54Mbps, dBm)
0xF8	TSSI off 5G TX power (54Mbps, dBm)

2.43 2G/5G ePAeLNA GPIO function (0x25, 0x35, 0x36)

1. 0x25[7:5]:

i. 010: Enable external RF component GPIO, like PAPE, LNA_EN, TRSW_P, TRSW_N

ii. 000 : Disable external RF component GPIO, like PAPE, LNA_EN, TRSW_P, TRSW_N

2. 0x35[1:0] : For 2.4 and 5GHz ePA setting
   i. 00: 2.4G+5G external PA mode
   ii. 01: 5G external PA mode
   iii. 10: 2.4G external PA mode
   iv. 11: disable mode
3. 0x36[2]: For 2.4GHz LNA setting
   i. 0: Board without external LNA for 2.4GHz band must set this bit to 0.
   ii. 1: Board with external LNA for 2.4GHz band must set this bit to 1 (default value).
4. 0x36[3]: For 5GHz LNA setting
   i. 0: Board without external LNA for 5GHz band must set this bit to 0.
   ii. 1: Board with external LNA for 5GHz band must set this bit to 1.