MT7603E
802.11 b/g/n Wi-Fi single chip EEPROM Content Programming guide

Version: 1.4
Release date: 2015-10-20

Document Revision History

Revision	Date	Author	Description
1.0	2014-05-13	AlexCC Lin	Formal released
1.1	2015-01-21	Li Yi-Yan	Add 0x43 descriptions 1. 0x43[6] for Shaping filter ON/OFF option 2. 0x43[7] for Dynamic PA switch ON/OFF option
1.2	2015-05-13	Li Yi-Yan	Add 0x55/0xF2 descritptions 1.0x55 is temperature sensor calibration 2.0xF2 is TSS off 2.4GHz Tx Power SKU(54M,OFDM)
1.3	2015-06-24	Li Yi-Yan	1. add Tx Temperature compensate description 0xC6~0xD7 2. add record factory calibration description 0x1B0
1.4	2015-10-20	Li Yi-Yan	1. Add control bit for PCIE big swing. 0x25[7] 0x25[7]=1, PCIE swing big. 0x25[7]=0, Default setting

Table of Contents

1 General Description

1.1 General Descriptions

The MT7603E EEPROM layout provides configuration for vendor/product ID, SW setting, RF TX power setting.

2 MT7603E EEPROM Layout

Offset	Default (hex)	b15 ~b8	b7 ~ b0
00h	7603	Chip ID	
02h	0100	EEPROM Version	
04h	FFFF	Mac Address [15:0]	
06h	FFFF	Mac Address [31:16]	
08h	FFFF	Mac Address [47:32]	
0Ah~32h	FFFF	ASIC Reserved*	
34h	3422	NIC Configuration 0	
36h	2000	NIC Configuration 1	
38h	FFFF	Country Region 2.4G band	ASIC Reserved*
3Ah	0100	LED Mode	ASIC Reserved*
3Ch	0000	ASIC Reserved*	
3Eh	0000	ASIC Reserved*	
40h	0000	ASIC Reserved*	
42h	0022	NIC Configuration 2	
44h	0000	ASIC Reserved*	ASIC Reserved*
46h	0000	ASIC Reserved*	ASIC Reserved*
48h	0000	ASIC Reserved*	ASIC Reserved*
4Ah	0000	ASIC Reserved*	ASIC Reserved*
4Ch	0000	ASIC Reserved*	ASIC Reserved*
4Eh	01E0	ASIC Reserved*	ASIC Reserved*
50h	0081	ASIC Reserved*	20M/40M BW Power delta for 2.4G band
52h	9400	ASIC Reserved *	ASIC Reserved*
54h	B040	ASIC Reserved*	ASIC Reserved*
56h	C940	TX0 2.4G PA TSSI offset	TX0 2.4G PA TSSI slope
58h	0027	TX0 2.4G TX power offset low	TX0 2.4G TX power
5Ah	0000	TX0 2.4G TX power offset high	TX0 2.4G TX power offset middle
5Ch	C940	TX1 2.4G PA TSSI offset	TX1 2.4G PA TSSI slope
5Eh	0027	TX1 2.4G TX power offset low	TX1 2.4G TX power
60h	0000	TX1 2.4G TX power offset high	TX1 2.4G TX power offset middle
9Ch~9Fh		Reserved	Reserved
A0h	C6C6	2.4G TX power for CCK 5.5M/11M	2.4G TX power for CCK 1M/2M

Offset	Default (hex)	b15 ~b8	b7 ~ b0
A2h	C4C4	2.4G TX power for OFDM 12M/18M	2.4G TX power for OFDM 6M/9M
A4h	C0C4	2.4G TX power for OFDM 48M	2.4G TX power for OFDM 24M/36M
A6h	C4C0	2.4G/5G TX power for HT MCS=0/8	2.4G TX power for OFDM 54M
A8h	C4C4	2.4G/5G TX power for HT MCS=1,2/9,10	2.4G/5G TX power for HT MCS=32
AAh	C0C4	2.4G/5G TX power for HT MCS=5/13	2.4G/5G TX power for HT MCS=3,4/11,12
ACh	C0C0	2.4G/5G TX power for HT MCS=7/15	2.4G/5G TX power for HT MCS=6,14
AEh	0000	Reserved	Reserved
B0h~F4h	0000	Reserved	Reserved
F4h	00BC	Xtal trim 2nd compensation	Frequence offset(Xtal trim)
F6h	8800	ASIC Reserved*	XTAL trim 3rd compensation
F8h	0000	Configured 2.4G Channels	ASIC Reserved*
FAh	0000	ASIC Reserved*	Configured 2.4G Channels
FFh~F8h	0000	ASIC Reserved*	ASIC Reserved*
110h~17Fh	0000	ASIC Reserved*	ASIC Reserved*
180h~1B7h	0000	Reserved	Reserved
1B8h~1BFh	0000	Reserved for Customer specific	Reserved for Customer specific

2.1 E2PROM layout version # (02h)

Value	Description
10h	Formal Version 1.0.
1 ~ 255	Invalid version. Treat as version 0.

2.2 NIC Configuration 0 (0x34)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		Board type		Reserved	External PA			TX Path setting				RX Path setting			
Reserved		Reserved		Reserved				1:1TX 2: 2TX				1: 1RX			
												2: 2RX			

NIC Configuration 0 Register Bit Fields Description

Offset	Field	Description
34h	3:0	RX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 RX front-end in the system.
		2 (0010): 2 RX front-end in the system. 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX front-end architecture in the system. 0 (0000): Reserved. 1 (0001): 1 TX front-end in the system.
		2 (0010): 2 TX front-end in the system. 3~ F (0011 ~ 1111): Reserved.
35h	9:8	external PA bit[8] : external 5G PA enable : 0 : disable, 1 : enable bit[9] : external 2.4G PA enable : 0 : disable, 1 : enable
	10	External PA current setting – the IO driving current setting for external PA control pin(PAPE) 1: 8 mA (default) 0: 16mA
	11	Reserved.

Offset	Field	Description
	13:12	Reserved for define the board type.
	15:14	Reserved.

2.3 NIC Configuration 1 (0x36)

Bit[7:0]=0xFF will be treated as INVALID and used Default Value.
Bit[15:8]=0xFF will be treated as INVALID and used Default Value

7	6	5	4	3	2	1	0
WPS PBC	5G side band for 40M BW	2.4G side band for 40M BW	Proprietary Test bit	WF1 AUX RX PATH SEL	WF0 AUX RX PATH SEL	Tx temp. scheme en	HW CTRL
0: off (D) 1: on	0: off(D) 1: on	0: off 1: on(D)	0: off(D) 1: on	0:off(D) 1: on	0:off(D) 1: on	0: off(D) 1: on	0: off(D) 1: on

15	14	13	12	11	10	9	8
DAC test bit	BT Coexist	TSSI Power compensation en	Antenna Diversity		Reserved	40M BW in 5G band	40M BW in 2.4G band
0: off (D) 1: on	0: off (D) 1: on	0: off(D) 1: on	00: Disable (D)			0: on (D) 1: off	0: on (D) 1: off

NIC Configuration 1 Register Bit Fields Description

Offset	Field	Description
36h	0	Hardware Radio Control. 0: disable hardware radio control (default value). 1: enable hardware radio control. When "hardware radio control" bit is enabled (=1), the driver will read MAC's GPIO13 status. When GPIO13 pin is low, the radio is disabled. When GPIO13 pin is high, the radio is enabled. The Radio ON/OFF is controlled by both software UI and MAC's GPIO pin.
	1	TX power temperature compensation scheme enable 0 : disable temperature compensation 1 : Enable temperature compensation This bit will disable/enable temperature compensation scheme. While this bit is enable, it means Tx power TSSI scheme is disabled (it must set 0x37 bit5 = 0) and using per-channel Tx ALC code scheme.

Offset	Field	Description
	2	WF0 Aux Rx path selection 0 : Use Main path Rx path, board select main rx path as rx data in. 1 : Use Aux Rx path, board select aux rx path as rx data in. In this mode, FW also refer 0xC0~0xC5 as external LNA gain setting.
	3	WF1 Aux Rx path selection 0 : Use Main path Rx path, board select main rx path as rx data in. 1 : Use Aux Rx path, board select aux rx path as rx data in. In this mode, FW also refer 0xC0~0xC5 as external LNA gain setting.
	4	Proprietary TEST BIT. For debug purpose. Default value is 0.
	5	2.4GHz side band for 40MHz BW. For debug purpose.
	6	5G side band for 40M BW For debug purpose.
	7	WPS Push Button Configuration control. 0: disable WPS PBC control (default value). 1: enable WPS PBC control. The WPS PBC function is controlled through GPIO[11]. If LED mode set to “Signal strength”(64), WPS PBC will be disabled.
37h	8	40M BW in 2.4GHz band. 0: enable 40MHz bandwidth for 2.4GHz band 1: disable 40MHz bandwidth for 2.4GHz band
	9	40M BW in 5G band 0: enable 40MHz bandwidth for 5GHz band. 1: disable 40MHz bandwidth for 5GHz band.
	10	Reserved
	12:11	Antenna Diversity control. Bit[12:11]: 00: disable diversity function (default value). *Not supported in 7603E
	13	TSSI power compensation enable 0 : disable TSSI power compensation , use per-channel ALC code 1 : enable TSSI power compensation, TSSI slop offset scheme. Note : When TSSI is enable , it’s not allowed to enable 36h[bit1].

Offset	Field	Description
	14	BT Coexist 0: Disable BT coexistence.
		1: Enable BT coexistence.
	15	DAC test bit 0: Disable DAC test.
		1: Enable DAC test.

2.4 Country Region Code for 2.4G band (0x39)

Default value = FFh, which means read from INF and registry, more flexible than reading from EEPROM, this is our current InstallShield CCS implementation. We do not recommend customers to read SKU from EEPROM. Value FFh is the default value.
CountryCode— Specify the domain code, can be FFh or one of the followings,

Index	Support Channels
0	CH 1 ~ 11
1	CH 1 ~ 13
2	CH 10 ~ 11
3	CH 10 ~ 13
4	CH 14
5	CH 1 ~ 14
6	CH 3 ~ 9
7	CH 5 ~ 13
30	Manual Channel (Refer to 0x118h~119h)
31	CH1 ~ 14 (CH1 ~ 11 active scan, CH12 ~ 14 passive scan)
32	CH1 ~ 13 (CH1 ~ 11 active scan, CH12 ~ 13 passive scan)
33	802.11b: CH1 to CH14 are active scan. 802.11g/n: CH1 to CH13 are active scan. CH14 is disallowed

Notes: If set to read SKU from EEPROM, only available if 2.4G Country Region code registers are programmed.

2.5 Frequency offset (0xF4/0xF5/0xF6)

Offset	Field	Description
F4h	6:0	Crystal trim code
	7	Crystal trim code valid bit 0 : non-valid , rom code will apply default value as crystal trim code 1: valid, rom code will apply 0xF4[6:0]'s value as crystal trim code.
F5h	5:0	Crystal trim code 2nd compensation value
	6	Crystal trim increase/decrease bit 0 : increase 1: decrease
	7	Crystal trim code 2nd compensation enable/disable bit 0 :disable 1: enable
F6h	5:0	Crystal trim code 3rd compensation value
	6	Crystal trim increase/decrease bit 0 : increase 1: decrease
	7	Crystal trim code 3rd compensation enable/disable bit 0 :disable 1: enable

0xF4 is used for MTK FT test only for crystal calibration-free feature .
MTK wafer manufactory used 0xF4, bit 0~6, to store frequency offset value which is measured under MTK FT environment. Each IC has each corresponding frequency offset .
Bit 7 of 0xF4 is used to enable to apply crystal code vale. "1" means enable and "0" means disablle. While Bit7 is 0 (disable), it means rom code will not use crystal value of 0xF4 but use crystal code default value in rom code. Default is "1" (enable).
0xF5/0xF6 is used for crystal re-calibration purpose in customer production line
If customers want to re-do frequency trimming in customer production line, please use 0xF5/F6 as second /third frequency offset. Rom/Firmware code will check 0xF5/0xF6 Bit7 to decide the crystal trim code need to be compensated or not. Here is the formula :

If (0xF4[7] == 1 && 0xF5[7] == 1 && 0xF6[7] == 1)
Final xtal trim code = 0xF4[6:0] +/- 0xF5[5:0] +/- 0xF6[5:0];
// the increase/descrease(+/-) depends on 0xF5/F6[6]'s value

Else if((0xF4[7] == 1 && 0xF5[7] == 1)
Final xtal trim code = 0xF4[6:0] +/- 0xF5[5:0];
Else if((0xF4[7] == 1)
Final xtal trim code = 0xF4[6:0];
Else
Use rom code default vale.

2.6 LED Mode Setting (0x3B)

Reserved.

2.7 NIC Configuration 2 (0x42)

Bit <15:13>	12	11	10:9	8	7	6	5	4	3	2	1	0
Co-exist stream mode	Reserved	Reserved	Xtal option	HW Ant Div	TX Stream 1: 1 Stream 2: 2 Stream				RX Stream 1: 1 Stream 2: 2 Stream			

Note:

1. The 1 stream support MCS0~MCS7. The 2 stream support MCS0~MCS15.
2. Stream setting should be equal or less than path setting of EEPROM (0x34)
3. Default=0xFF means that based on the path setting (0x34) for MAX capability.

NIC Configuration 2 Register Bit Fields Description

Offset	Field	Description
42h	3:0	RX stream. 0 (0000): Reserved 1 (0001): 1 RX stream 2 (0010): 2 RX stream 3 ~ F (0011 ~ 1111): Reserved.
	7:4	TX stream. 0 (0000): Reserved 1 (0001): 1 TX stream 2 (0010): 2 TX stream 3 ~ F (0011 ~ 1111): Reserved.

Offset	Field	Description
43h	8	HW Antenna Diversity 0 : Disable 1: Enable *not support in 7603
	10:9	Reserved
	11	Reserved.
	13:12	Reserved.
	14	Sharp filter enable 0:sharp shaping type 1:flat shaping type default : 0
	15	PA cell setting 1:Apply dynamic PA cell 0:Apply fixed Supper PA cell default : 0

2.8 20M/40M BW Power Delta for 2.4GHz (0x50h)

Driver compensates the TX power value of 40M BW with this configured value. (unit : 0.5dm)

TX power delta configuration Register Bit Fields Description

Offset	Field	Description
50h	5:0	40M BW TX power delta value (MAX=4dBm).(2.4G) 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101: 2.5dBm 000110: 3dBm 000111: 3.5dBm 001000: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.

	7	1: enableTX power compensation.
0x51h	5:0	40M BW TX power delta value (MAX=4dBm).(5G) 000001: 0.5dBm 000010: 1dBm 000011: 1.5dBm 000100: 2dBm 000101: 2.5dBm 000110: 3dBm 000111: 3.5dBm 001000: 4dBm
	6	1: increase 40M BW TX power with the delta value. 0: decrease 40M BW TX power with the delta value.
	7	1: enableTX power compensation.

Example:

The default calibrated TX power as followings with the TX power delta configuration is not enable.

- 40M BW TX power= 14dBm and 20M BW TX power = 14dBm

If want keep 20M BW TX power in 14dBm and reduce 40M BW TX power to 10dBm (delta=4dBm), set 50h = 88h (1000 1000).

2.9 2.4G Tx0 Power Slope /offset (0x56h~0x57h)

Driver compares current TSSI value with this TSSI reference value as a base to decide if real-time TX power compensation is required. 0xFF will be treated as invalid value. This function is controlled by 'external TX ALC' bit (NIC configuration1 bit1) or 'internal TX ALC ' bit (NIC configuration1 bit13).

2.10 2.4G Tx0 Target Power (0x58h)

It defines the TX0/TX1 2.4G target power at 54M. 1step = 0.5dB.

2.11 2.4G Tx0 Power low/middle/high Channel (59h~5Bh)

0x59~0x5B are used as channel TX power compensation in customer production line.

Customers could set different TX power compensation value according to different PCB design to reach flatter power responds.
For example
If customers found PCB had 1.5dB higher power variation in low channels and 1.5dB lower power variation in high channels.
Customer could use channel compensation offset to get flatter performance like setting as below.

Offset	Description	7	6	5	4	3	2	1	0

Offset	Description	7	6	5	4	3	2	1	0
59h~5Bh	Description	Power compensation enable bit 0 : disable 1 : enable	1: increase Tx power with the delta value 0:decrease Tx power with the delta value	Power delta related to origin target power Unit : 0.5dB					
0x59	TX0 2.4G Tx power offset low (CH1~5)(delta,dB)	0x83=> means SW will decrease 3 step(around -1.5dB) corresponding to TX0 2.4G TX power setting.							
0x5A	TX0 2.4G Tx power offset middle (CH6~10)(delta,dB)	0x80=> means SW will decrease 0 step(around 0dB) corresponding to TX0 2.4G TX power setting.							
0x5B	TX0 2.4G Tx power offset high (CH11~14)(delta,dB)	0xC3=> means SW will increase 3 step(around +1.5dB) corresponding to TX0 2.4G TX power setting.							

2.12 2.4G Tx1 Power Slope /offset (0x5Ch~0x5Dh)

The same description of 2.4G Tx0 PowerSlop/offset but it's Tx1 setting.

2.13 2.4G Tx1 Power offset low/middle/high Channel(0x5Fh~0x61h)

The same description of Tx0 Power offset low/middle/high but it's Tx1 setting.

2.14 2.4G Tx rate power configuration (0xA0h~0xBFh)

Default value=0x00, 6bit signed 2's complement value. (1 step=0.5dBm)
0xA0~0xBE are used as TX rate power configuration in customer production line.
Customers could set different TX rate power according to different RF power requirement.

Offset	Field	Description
A0h ~BFh	5:0	Tx per-rate power setting
	7:6	Bit[7] : enable Bit[6] : 0 : decrease , 1 :increase

The 1 step=0.5dBm.

Each Field in Bit	Description
7	Power compensation enable bit 0 : disable 1 : enable
6	1: increase TX power with the delta value. 0: decrease TX power with the delta value.

Offset	Default Value	Description	Bit [5:0]
A0h	C6	2G TX power for CCK 1M/2M	TX power setting
A1h	C6	2G TX power for CCK 5.5M/11M	TX power setting
A2h	C4	2G TX power for OFDM 6M/9M	TX power setting
A3h	C4	2G TX power for OFDM 12M/18M	TX power setting
A4h	C4	2G TX power for OFDM 24M/36M	TX power setting
A5h	C0	2G TX power for OFDM 48M	TX power setting
A6h	C0	2G TX power for OFDM 54M	TX power setting
A7h	C4	2G TX power for HT/VHT MCS=0/8	TX power setting
A8h	C4	2G TX power for HT/VHT MCS=32	TX power setting
A9h	C4	2G TX power for HT/VHT MCS=1,2/9,10	TX power setting
AAh	C4	2G TX power for HT MCS=3,4/11,12	TX power setting
ABh	C0	2G TX power for HT MCS=5/13	TX power setting
ACh	C0	2G TX power for HT MCS=6/14	TX power setting
ADh	C0	2G TX power for HT MCS=7/15	TX power setting

Example:

If the table content is :

Offset	Ex. Value	Description	Example description
A0h	C3	2G TX power for CCK 1M/2M	0xC3=> 2G 1~11M & 6~18M will have 1.5dB higher power than 54M. 0x00=> 2G 24~54M will have equal power with 54M.
A1h	C3	2G TX power for CCK 5.5M/11M	
A2h	C3	2G TX power for OFDM 6M/9M	
A3h	C3	2G TX power for OFDM 12M/18M	
A4h	0	2G TX power for OFDM 24M/36M	
A5h	0	2G TX power for OFDM 48M	
A6h	0	2G TX power for OFDM 54M	
A7h	C2	2G TX power for HT/VHT MCS=0/8	0xC2 => 2G HT MCS0~3 &MCS8~11 will have 1dB higher power than 54M. 0x82 => 2G HT MCS4~7 &MCS12~15 will have 1dB lower power than 54M. 0xC2=> 5G HT MCS0~3 &MCS8~11 will have 1dB higher power than 54M. 5G VHT MCS0~3 will have 1dB higher power than 54M. 0x82=> 5G HT MCS4~7 &MCS12~15 will have 1dB lower power than 54M. 5G VHT MCS4~7 will have 1dB lower power than 54M.
A8h	C2	2G TX power for HT/VHT MCS=32	
A9h	82	2G TX power for HT/VHT MCS=1,2/9,10	
AAh	82	2G TX power for HT/VHT MCS=3,4/11,12	
ABh	C2	2G TX power for HT MCS=5/13	
ACh	C2	2G TX power for HT MCS=6/14	
ADh	82	2G TX power for HT MCS=7/15	

2.15 Reserved for Customer (0x1B8h~0x1BFh)

2.16 Configured 2.4G Channels (0xB0h~B1h)

Default value=0x00, this field is available when 0x39h = 30d. (Configured channel)

7	6	5	4	3	2	1	0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

15	14	13	12	11	10	9	8
Reserve	Reserve	CH14	CH13	CH12	CH11	CH10	CH9
0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on	0: off 1: on

For example:

If available channels are 1,2,3 and 5, then

0x39h = 30d, 0x118h = 17h, 0x119h = 00h.

2.17 TSSI OFF 2.4GHz Tx Power SKU (0xF2h)

Unit: 0.5dBm

Driver will use this value as reference target power of SKU function.

TSSI off:

If 54M target power is 13dBm, 13dBm= 13*2 = 26(dec) = 0x1A(hex)

0XF2 offset should be filled with 0x1A value.

2.18 Temperature sensor calibration (0x55h)

For K-free IC, thermal sensor calibration value will be filled in MTK FT production line.

Offset	Field	Description
0x55h	6:0	MTK FT Thermal sensor value
	7	1: Use temperature sensor calibration value 0: Not use temperature sensor calibration value

2.19 Record factory calibration (0x1B0h)

Reserved for Customer record factory calibration.

2.20 Tx Thermal Compensation (0xC6h~0xD7h)

Offset	Description
0xC6	-7 step boundary
0xC7	-6 step boundary

0xC8	-5 step boundary
0xC9	-4 step boundary
0xCA	-3 step boundary
0xCB	-2 step boundary
0xCC	-1 step boundary
0xCD	-0 step boundary
0xCE	Compensate reference step Reference step can be used scale of 0.5 or 1dB for compensated power. CEh[0]==0 step is 0.5dBm, CEh[0]==1 step is1dBm.
0xCF	2.4G reference temp
0xD0	+1 step boundary
0xD1	+2 step boundary
0xD2	+3 step boundary
0xD3	+4 step boundary
0xD4	+5 step boundary
0xD5	+6 step boundary
0xD6	+7 step boundary
0xD7	Reserved

+1 Step means that the transmission power will be compensated +1 dB after thermal ADC value exceeding boundary..

Ex. CEh[0]=0, then CCh[7:0] means" TX power -0.5dB boundary"

Note: MUST fill a constant value to the unused threshold. For the low temperature, please fill 0x00. For the high temperature, please fill 0x7F.

Ex:

Temp (°C)	ADC value	TX Power (dBm)	Power Difference with +25°C	Power Compensation Value
		11g 54Mbps		
-40	1F	25.5	+3	-3
-10	29	24.5	+2	-2
0	32	23.5	+1	-1
25	3E	22.5	0	0
45	47	21.5	-1	+1
65	51	20.5	-2	+2
85	5D	19.5	-3	+3

Offset	b15 ~b8 (ALC)		b7 ~ b0 (ALC)	
C6h	TX power -6 TSSI boundary	00	TX power -7 TSSI boundary	00
C8h	TX power -4 TSSI boundary	00	TX power -5 TSSI boundary	00
CAh	TX power -2 TSSI boundary	29	TX power -3 TSSI boundary	1F
CCh	TX power +0 TSSI boundary	3E	TX power -1 TSSI boundary	32
CEh	2.4G reference temp		2.4G reference step	01
D0h	TX power +2 TSSI boundary	51	TX power +1 TSSI boundary	47

D2h	TX power +4 TSSI boundary	7F	TX power +3 TSSI boundary	5D
D4h	TX power +6 TSSI boundary	7F	TX power +5 TSSI boundary	7F
D6h	Reserved		TX power +7 TSSI boundary	7F

2.21 Config1 option (0x25h)

For PCIE Swing change

Offset	Field	Description
0x25h	7	1: Use big PCIE Swing for eye diagram. 0: Use default setting.